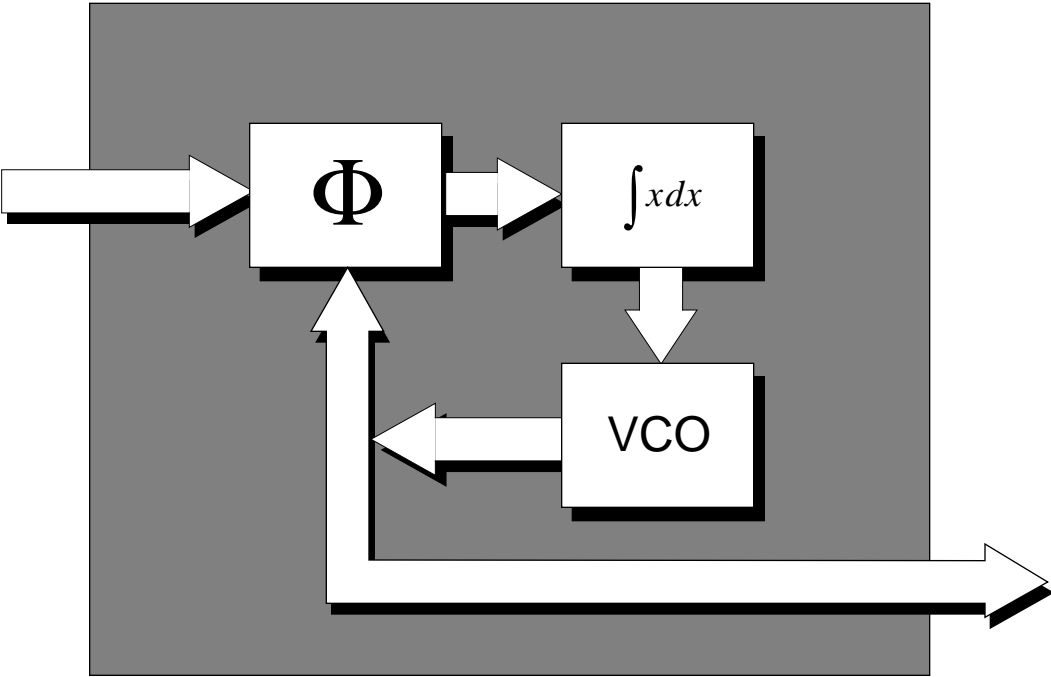


SECTION 9 PLL CLOCK OSCILLATOR



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9.1 PLL CLOCK OSCILLATOR INTRODUCTION

The DSP56K family of processors (with the exception of the DSP56000 and DSP56001) features a PLL (phase-locked loop) clock oscillator in its central processing module, shown in Figure 9-2. The PLL allows the processor to operate at a high internal clock frequency using a low frequency clock input, a feature which offers two immediate benefits. Lower frequency clock inputs reduce the overall electromagnetic interference generated by a system, and the ability to oscillate at different frequencies reduces costs by eliminating the need to add additional oscillators to a system.

The PLL performs frequency multiplication to allow the processor to use almost any available external system clock for full speed operation, while also supplying an output clock synchronized to a synthesized internal core clock. It also improves the synchronous timing of the processor's external memory port, significantly reducing the timing skew between EXTAL and the internal chip phases. The PLL is unusual in that it provides a low power divider on its output, which can reduce or restore the chip operating frequency without losing the PLL lock

A DSP56K processor uses a four-phase clock for instruction execution which runs at the instruction execution rate. It can accept an external clock through the EXTAL input, or it can run on an internal oscillator, bypassing the PLL function, when the user connects an external crystal between XTAL and EXTAL. (The PLL need not be disabled when the processor accepts an external clock.)

9.2 PLL COMPONENTS

The PLL block diagram is shown below in Figure 9-1. The components of the PLL are described in the following sections.

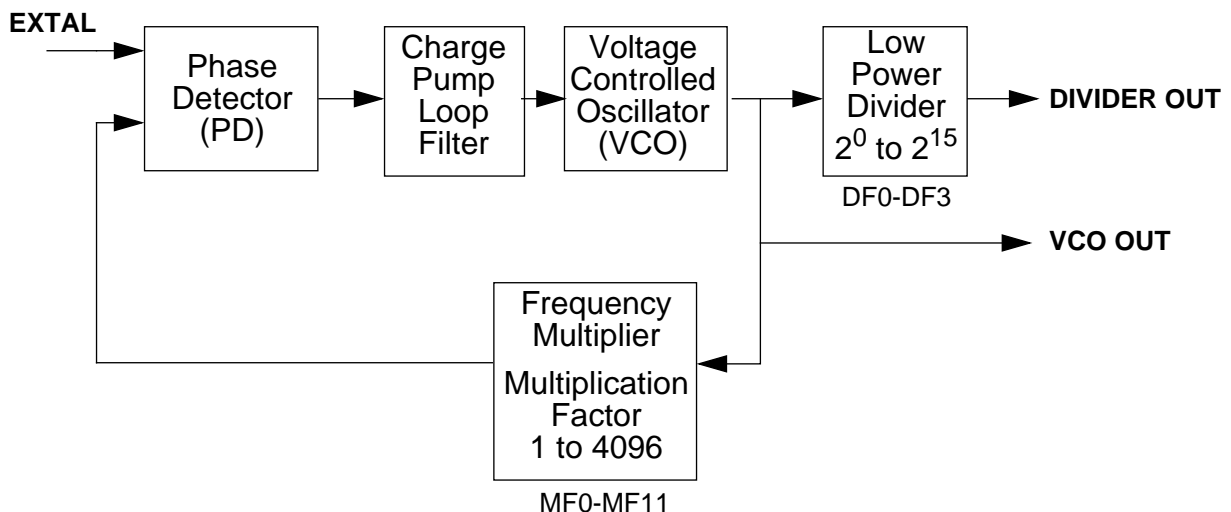


Figure 9-1 PLL Block Diagram

PLL COMPONENTS

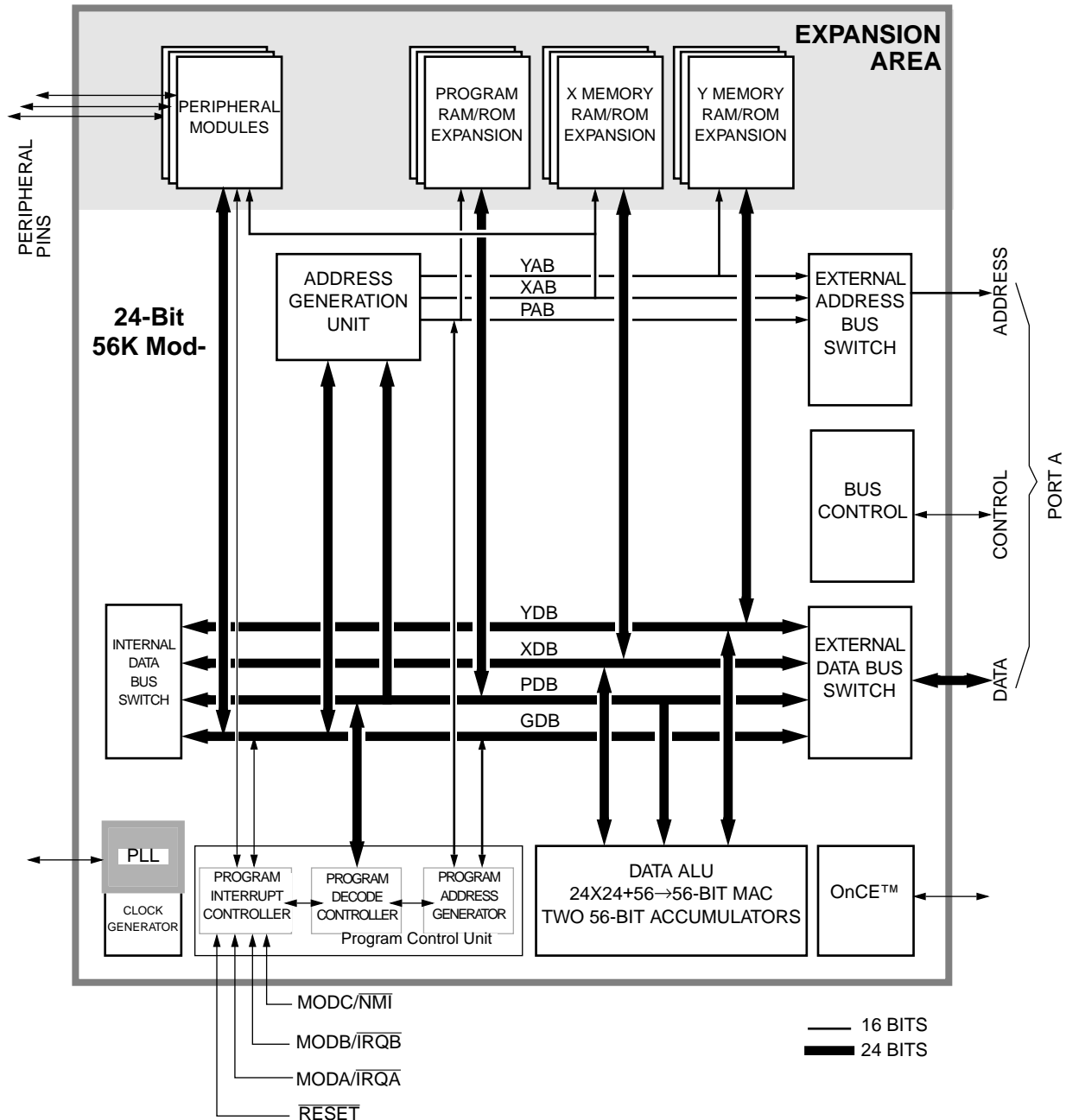


Figure 9-2 DSP56K Block Diagram

9.2.1 Phase Detector and Charge Pump Loop Filter

The Phase Detector (PD) detects any phase difference between the external clock (EXTAL) and an internal clock phase from the frequency multiplier. At the point where there is negligible phase difference and the frequency of the two inputs is identical, the PLL is in the “locked” state.

The charge pump loop filter receives signals from the PD, and either increases or decreases the phase based on the PD signals. An external capacitor is connected to the PCAP pin (described in Section 9.3) and determines the PLL operation. (See the appropriate Technical Data Sheet for more detailed information about a particular device's phase and frequency.)

After the PLL locks on to the proper phase/frequency, it reverts to the narrow bandwidth mode, which is useful for tracking small changes due to frequency drift of the EXTAL clock.

9.2.2 Voltage Controlled Oscillator (VCO)

The VCO can oscillate at frequencies from the minimum speed specified in a device's Technical Data Sheet (typically 10 MHz) up to the device's maximum allowed clock input frequency.

9.2.3 Frequency Multiplier

Inside the PLL, the frequency multiplier divides the VCO output frequency by its division factor (n). If the frequency multiplier's output frequency is different from the EXTAL frequency, the charge pump loop filter generates an error signal. The error signal causes the VCO to adjust its frequency until the two input signals to the phase detector have the same phase and frequency. At this point (phase lock) the VCO will be running at n times the EXTAL frequency, where n is the multiplication factor for the frequency multiplier. The programmable multiplication factor ranges from 1 to 4096.

9.2.4 Low Power Divider (LPD)

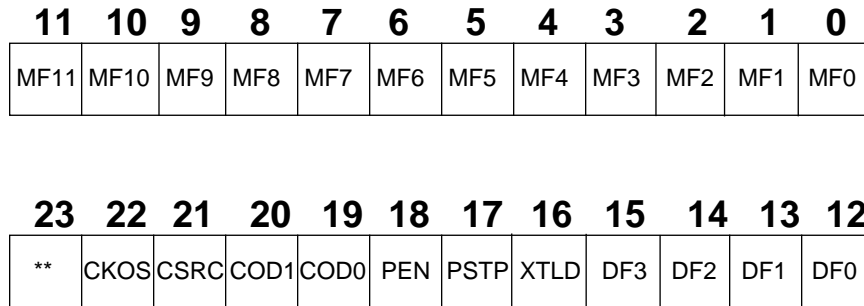
The Low Power Divider (LPD) divides the output frequency of the VCO by any power of 2 from 2^0 to 2^{15} . Since the LPD is not in the closed loop of the PLL, changes in the divide factor will not cause a loss of lock condition. This fact is particularly useful for utilizing the LPD in low power consumption modes when the chip is not involved in intensive calculations. This can result in significant power saving. When the chip is required to exit the low power mode, it can immediately do so with no time needed for clock recovery or PLL lock.

9.2.5 PLL Control Register (PCTL)

The PLL control register (PCTL) is a 24-bit read/write register which directs the operation of the on-chip PLL. It is mapped into the processor's internal X memory at X:\$FFFD. The PCTL control bits are described in the following sections.

9.2.5.1 PCTL Multiplication Factor Bits (MF0-MF11) - Bits 0-11

The Multiplication Factor Bits MF0-MF11 define the multiplication factor (MF) that will be applied to the PLL input frequency. The MF can be any integer from 1 to 4096. Table 9-1



** Reserved bits, read as zero, should be written with zero for future compatibility.

Figure 9-3 PLL Control Register (PCTL)

shows how to program the MF0-MF11 bits. The VCO will oscillate at a frequency of $MF \times F_{ext}$, where F_{ext} is the EXTAL clock frequency. The multiplication factor must be chosen to ensure that the resulting VCO output frequency will lay in the range specified in the device's Technical Data Sheet. Any time a new value is written into the MF0-MF11 bits, the PLL will lose the lock condition. After a time delay, the PLL will relock. The MF0-MF11 bits are set to a pre-determined value during hardware reset; the value is implementation dependent and may be found in each DSP56K family member's user manual.

Table 9-1 Multiplication Factor Bits MF0-MF11

MF11-MF0	Multiplication Factor MF
\$000	1
\$001	2
\$002	3
•	•
•	•
\$FFE	4095
\$FFF	4096

9.2.5.2 PCTL Division Factor Bits (DF0-DF3) - Bits 12-15

The Division Factor Bits DF0-DF3 define the divide factor (DF) of the low power divider. These bits specify any power of two divide factor in the range from 2^0 to 2^{15} . Table 9-2

shows the programming of the DF0-DF3 bits. Changing the value of the DF0-DF3 bits will not cause a loss of lock condition. Whenever possible, changes of the operating frequency of the chip (for example, to enter a low power mode) should be made by changing the value of the DF0-DF3 bits rather than changing the MF0-MF11 bits. For $MF \leq 4$, changing DF0-DF3 may lengthen the instruction cycle following the PLL control register update; this is done in order to keep synchronization between EXTAL and the internal chip clock. For $MF > 4$ such synchronization is not guaranteed and the instruction cycle is not lengthened. Note that CKOUT is synchronized with the internal clock in all cases. The DF bits are cleared (division by one) by hardware reset.

Table 9-2 Division Factor Bits DF0-DF3

DF3-DF0	Division Factor DF
\$0	2^0
\$1	2^1
\$2	2^2
•	•
•	•
\$E	2^{14}
\$F	2^{15}

9.2.5.3 PCTL XTAL Disable Bit (XTLD) - Bit 16

The XTAL Disable (XTLD) bit controls the on-chip crystal oscillator XTAL output. When XTLD is cleared, the XTAL output pin is active permitting normal operation of the crystal oscillator. When XTLD is set, the XTAL output pin is held in the high (“1”) state, disabling the on-chip crystal oscillator. If the on-chip crystal oscillator is not used (EXTAL is driven from an external clock source), it is recommended that XTLD be set (disabling XTAL) to minimize RFI noise and power dissipation. The XTLD bit is cleared by hardware reset.

9.2.5.4 PCTL STOP Processing State Bit (PSTP) - Bit 17

The PSTP bit controls the behavior of the PLL and of the on-chip crystal oscillator during the STOP processing state. When PSTP is set, the PLL and the on-chip crystal oscillator will remain operating while the chip is in the STOP processing state, enabling rapid recovery from the STOP state. When PSTP is cleared, the PLL and the on-chip crystal oscillator will be disabled when the chip enters the STOP processing. For minimal power consumption during the STOP state, at the cost of longer recovery time, PSTP should be

cleared. To enable rapid recovery when exiting the STOP state, at the cost of higher power consumption in the STOP state, PSTP should be set. PSTP is cleared by hardware reset.

9.2.5.5 PCTL PLL Enable Bit (PEN) - Bit 18

The PEN bit enables the PLL operation. When this bit is set, the PLL is enabled and the internal clocks will be derived from the PLL VCO output. When this bit is cleared, the PLL is disabled and the internal clocks are derived directly from the clock connected to the EXTAL pin. When the PLL is disabled, the VCO does not operate in order to minimize power consumption. The PLOCK pin is asserted when PEN is cleared. The PEN bit may be set by software but it cannot be reset by software. During hardware reset this bit receives the value of the PINIT pin. The only way to clear PEN is to hold the PINIT pin low during hardware reset.

A relationship exists between PSTP and PEN where PEN adjusts PSTP’s control of the PLL operation. When PSTP is set and PEN (see Table 9-3) is cleared, the on-chip crystal oscillator remains operating in the STOP state, but the PLL is disabled. This power saving feature enables rapid recovery from the STOP state when the user operates the chip with an on-chip oscillator and with the PLL disabled.

Table 9-3 PSTP and PEN Relationship

		Operation during STOP			
PSTP	PEN	PLL	Oscillator	Recovery	Power Consumption
0	x	Disabled	Disabled	long	minimal
1	0	Disabled	Enabled	rapid	lower
1	1	Enabled	Enabled	rapid	higher

9.2.5.6 PCTL Clock Output Disable Bits (COD0-COD1) - Bits 19-20

The COD0-COD1 bits control the output buffer of the clock at the CKOUT pin. Table 9-4 specifies the effect of COD0-COD1 on the CKOUT pin. When both COD0 and COD1 are set, the CKOUT pin is held in the high (“1”) state. If the CKOUT pin is not connected to external circuits, it is recommended that both COD1 and COD0 be set (disabling clock output) to minimize RFI noise and power dissipation. If the CKOUT output is low at the moment the COD0-COD1 bits are set, it will complete the low cycle and then be disabled high. If the programmer re-enables the CKOUT output before it reaches the high logic level during the disabling process, the CKOUT operation will be unaffected. The COD0-COD1 bits are cleared by hardware reset.

Table 9-4 Clock Output Disable Bits COD0-COD1

COD1	COD0	CKOUT Pin
0	0	Clock Out Enabled, Full Strength Output Buffer
0	1	Clock Out Enabled, 2/3 Strength Output Buffer
1	0	Clock Out Enabled, 1/3 Strength Output Buffer
1	1	Clock Out Disabled

9.2.5.7 PCTL Chip Clock Source Bit (CSRC) - Bit 21

The CSRC bit specifies whether the clock for the chip is taken from the output of the VCO or is taken from the output of the Low Power Divider (LPD). When CSRC is set, the clock for the chip is taken from the VCO. When CSRC is cleared, the clock for the chip is taken from the output of the LPD. See Section 9.4.8 for restrictions. CSRC is cleared by hardware reset.

9.2.5.8 PCTL CKOUT Clock Source Bit (CKOS) - Bit 22

The CKOS bit specifies whether the CKOUT clock output is taken from the output of the VCO or is taken from the output of the Low Power Divider (LPD). When CKOS is set, the CKOUT clock output is taken from the VCO. When CKOS is cleared, the CKOUT clock output is taken from the output of the LPD. If the PLL is disabled (PEN=0), CKOUT is taken from EXTAL. See Section 9.4.8 for restrictions. CKOS is cleared by hardware reset.

9.2.5.9 PCTL Reserved Bit - Bit 23

This bit is reserved for future expansion. It reads as zero and should be written with zero for future compatibility.

9.3 PLL PINS

Some of the PLL pins need not be implemented. The specific PLL pin configuration for each DSP56K chip implementation is available in the respective device's user's manual. The following pins are dedicated to the PLL operation:

- PVCC** VCC dedicated to the analog PLL circuits. The voltage should be well regulated and the pin should be provided with an extremely low impedance path to the VCC power rail. PVCC should be bypassed to PGND by a 0.1µF capacitor located as close as possible to the chip package.
- PGND** GND dedicated to the analog PLL circuits. The pin should be provided with an extremely low impedance path to ground. PVCC should be bypassed to PGND by a 0.1µF capacitor located as close as possible to the chip package.

- CLVCC** VCC for the CKOUT output. The voltage should be well regulated and the pin should be provided with an extremely low impedance path to the VCC power rail. CLVCC should be bypassed to CLGND by a 0.1 μ F capacitor located as close as possible to the chip package.
- CLGND** GND for the CKOUT output. The pin should be provided with an extremely low impedance path to ground. CLVCC should be bypassed to CLGND by a 0.1 μ F capacitor located as close as possible to the chip package.
- PCAP** Off-chip capacitor for the PLL filter. One terminal of the capacitor is connected to PCAP while the other terminal is connected to PVCC. The capacitor value is specified in the particular device's Technical Data Sheet.
- CKOUT** This output pin provides a 50% duty cycle output clock synchronized to the internal processor clock when the PLL is enabled and locked. When the PLL is disabled, the output clock at CKOUT is derived from, and has the same frequency and duty cycle as, EXTAL.
- Note:** If the PLL is enabled and the multiplication factor is less than or equal to 4, then CKOUT is synchronized to EXTAL.
- CKP** This input pin defines the polarity of the CKOUT signal. Strapping CKP through a resistor to GND will make the CKOUT polarity the same as the EXTAL polarity. Strapping CKP through a resistor to VCC will make the CKOUT polarity the inverse of the EXTAL polarity. The CKOUT clock polarity is internally latched at the end of the hardware reset, so that any changes of the CKP pin logic state after deassertion of $\overline{\text{RESET}}$ will not affect the CKOUT clock polarity.
- PINIT** During the assertion of hardware reset, the value at the PINIT input pin is written into the PEN bit of the PLL control register. After hardware reset is deasserted, the PINIT pin is ignored.
- PLOCK** The PLOCK output originates from the Phase Detector. The chip asserts PLOCK when the PLL is enabled and has locked on the proper phase and frequency of EXTAL. The PLOCK output is deasserted by the chip if the PLL is enabled and has not locked on the proper phase and frequency. PLOCK is asserted if the PLL is disabled. PLOCK is a reliable indicator of the PLL lock state only after exiting the hardware reset state.

9.4 PLL OPERATION CONSIDERATIONS

The following paragraphs discuss PLL operation considerations.

9.4.1 Operating Frequency

The operating frequency of the chip is governed by the frequency control bits in the PLL control register as follows:

$$F_{\text{CHIP}} = \frac{F_{\text{EXT}} \times \text{MF}}{\text{DF}} = \frac{F_{\text{VCO}}}{\text{DF}}$$

where: DF is the division factor defined by the DF0-DF3 bits

F_{CHIP} is the chip operating frequency

F_{EXT} is the external input frequency to the chip at the EXTAL pin

F_{VCO} is the output frequency of the VCO

MF is the multiplication factor defined by the MF0-MF11 bits

The chip frequency is derived from the output of the low power divider. If the low power divider is bypassed, the equation is the same but the division factor should be assumed to be equal to one.

9.4.2 Hardware Reset

Hardware reset causes the initialization of the PLL. The following considerations apply:

1. The MF0-MF11 bits in the PCTL register are set to their pre-determined hardware reset value. The DF0-DF3 bits and the Chip Clock Source bit in the PCTL register are cleared. This causes the chip clock frequency to be equal to the external input frequency (EXTAL) multiplied by the multiplication factor defined by MF0-MF11.
2. During hardware reset assertion, the PINIT pin value is written into the PEN bit in the PCTL register. If the PINIT pin is asserted (setting PEN), the PLL acquires the proper phase/frequency. While hardware reset is asserted, the internal chip clock will be driven by the EXTAL pin until the PLL achieves lock (if enabled). If the PINIT pin is deasserted during hardware reset assertion, the PEN bit is cleared, the PLL is deactivated and the internal chip clock is driven by the EXTAL pin.
3. PLOCK is a reliable indicator of the PLL lock state only after exiting the hardware reset state.

4. For all input frequencies which would result in a VCO output frequency lower than the minimum specified in the device's Technical Data Sheet (typically 10 MHz), PINIT must be cleared during hardware reset, disabling PLL operation. Otherwise, proper operation of the PLL cannot be guaranteed. If the resulting VCO clock frequency would be less than the minimum and the user wishes to operate with the PLL enabled, the user must issue an instruction which loads the PCTL control register with a multiplication factor that would bring the VCO frequency above 10 MHz and would enable the PLL operation. Until this instruction is executed, the PLL is disabled, which may cause a large skew (<15nsec) between the external input clock and the internal processor clock. If internal low frequency of operation is desired with the PLL enabled, the VCO output frequency may be divided down by using the internal low power divider.
5. The CKP pin only affects the CKOUT clock polarity during the hardware reset state. At the end of the hardware reset state, the CKP state is internally latched.

9.4.3 Operation with PLL Disabled

1. If the PLL is disabled, the PLOCK pin is asserted.
2. If the PLL is disabled, the internal chip clock and CKOUT are driven from the EXTAL input.

9.4.4 Changing the MF0-MF11 Bits

Changes to the MF0-MF11 bits cause the following to occur:

1. The PLL will lose the lock condition, the PLOCK pin will be deasserted.
2. The PLL acquires the proper phase/frequency. Until this occurs the internal chip clock phases will be frozen. This ensures that the clock used by the chip is a clock that has reached a stable frequency.
3. When lock occurs, PLOCK is asserted and the PLL drives the internal chip clock and CKOUT.
4. While PLL has not locked, CKOUT is held low if CKP is cleared. CKOUT is held high if CKP is set.

9.4.5 Change of DF0-DF3 Bits

Changes to the DF0-DF3 bits do not cause a loss of lock condition. The internal clocks will immediately revert to the frequency prescribed by the new divide factor. For $MF \leq 4$, changing DF0-DF3 may lengthen the instruction cycle or CKOUT pulse following the PLL control register update in order to keep synchronization between EXTAL and the internal

chip clock. (Here, T_3 is equal to the phase described by the new divide factor plus the time required to wait for a synchronizing pulse, which is less than $1.5ET_c$.) For $MF > 4$, such synchronization is not guaranteed and the instruction cycle is not lengthened.

If the DF0-DF3 bits are changed by the same instruction that changes the MF0-MF11 bits, the LPD divider factor changes before the detection of the change in the multiplication factor. This means that the detection of loss of lock will occur after the LPD has started dividing by the new division factor.

9.4.6 Loss of Lock

The PLL distinguishes between cases where $MF > 4$ and cases where $MF \leq 4$. If $MF \leq 4$, the PLL will detect loss of lock if a skew of 2.5 to 4.5 ns develops between the two clock inputs to the phase detector.

If $MF > 4$, the PLL will detect loss of lock when there is a discrepancy of one clock cycle between the two clock inputs to the phase detector. When either of these two conditions occurs, the following also occur:

1. PLOCK will be deasserted, indicating that loss of lock condition has occurred.
2. The PLL will re-acquire the proper phase/frequency. When lock occurs, PLOCK will be asserted.

9.4.7 STOP Processing State

If the PSTP bit is cleared, executing the STOP instruction will disable the on-chip crystal oscillator and the PLL. In this state the chip consumes the least possible power. When recovering from the STOP state, the recovery time will be 16 or 64k external clock cycles (according to bit 6 in the Operating Mode Register) plus the time needed for the PLL to achieve lock.

If the PSTP bit is set, executing the STOP instruction will leave the on-chip crystal oscillator (if XTLD=0) and the PLL loop (if PEN=1) operating, but will disable the clock to the LPD and the rest of the DSP. When recovering from the STOP state, the recovery time will be only three clock cycles.

9.4.8 CKOUT Considerations

The CKOUT clock output is held high while disabled, which is also while the COD0-COD1 bits are set. If the CKOUT clock output is low at the moment the COD0-COD1 bits are set, then the CKOUT clock output will complete the low cycle and then be disabled high. If the programmer re-enables the CKOUT clock output before it reaches the high logic level during the disabling process, the CKOUT operation will be unaffected.

While the PLL is regaining lock, the CKOUT clock output remains at the same logic level it held when the PLL lost lock, which is when the clocks were frozen in the DSP.

When the chip enters the WAIT processing state, the core phases are disabled but CKOUT continues to operate. When PLL is disabled, CKOUT will be fed from EXTAL.

If $DF > 1$ and $CKOS \neq CSRC$, then the programmer must change either CKOS or CSRC before taking any action that causes the PLL to lose and subsequently regain lock, such as changing the multiplication factor, enabling PLL operation, or recovering from the STOP state with $PSTP = 0$.

Any change of the CKOS or CSRC bits must be done while $DF = 1$.

9.4.9 Synchronization Among EXTAL, CKOUT, and the Internal Clock

Low clock skew between EXTAL and CKOUT is guaranteed only if $MF \leq 4$. The synchronization between CKOUT and the internal chip activity and Port A timing is guaranteed in all cases where $CKOS = CSRC$ and the bits have never differed from one another.