79RC5000 Document Errata

Notes

Supplemental Information

This Document Errata reflects all changes found in the April 1998 version of the *IDT79RC5000 RISC Microprocessor Reference Manual,* Version 1.1 and the data sheet for this device.

Revision History

February 1999: First version of documentation errata for this device.

September 15, 1999: Added Item #2.

September 17, 1999: Changed pin 66 to pin 63 in Item #2.

September 26, 2000: Added Items #3 and 4.

Errata Items

Item #1 - Changes to Boot-Mode settings for bits 20, 33 and 37 in Table 14.1 on page 14-4 of manual.

Issue: In the Boot-Mode settings Table 14.1, bits 18:255 are noted as Reserved: Must be zero. Changes to the settings listed for bits 20, 33, and 37 in the documentation should be reflected as follows:

Bit	Value	Mode Setting
0	Reserved: must be zero	
1:4	XmitDatPat: System interface data rate for block writes only	
	0	DDDD
	1	DDxDDx
	2	DDxxDDxx
	3	DxDxDxDx
	4	DDxxxDDxxx
	5	DDxxxxDDxxxx
	6	DxxDxxDxxDxx
	7	DDxxxxxxDDxxxxxx
	8	DxxxDxxxDxxxDxxx
	9:15	Reserved

Bit	Value	Mode Setting
5:7	SysCkRatio: Pclock to SysClock Multiplier.	
	0	Multiply by 2
	1	Multiply by 3
	2	Multiply by 4
	3	Multiply by 5
	4	Multiply by 6
	5	Multiply by 7
	6	Multiply by 8
	7	Reserved
8	EndBit: Specifies byte ordering. Logically ORed with the BigEndian signal.	
	0	Little-Endian
	1	Big Endian
9:10	Non-Block Write: Determines how non-block writes are handled.	
	0	R4x00 compatible
	1	Reserved
	2	Pipelined writes
	3	Write-reissue
11	TmrIntEn: Disables Timer Interrupt on Int*[5]	
	0	Timer Interrupt Enabled
	1	Timer Interrupt Disabled
12	Secondary Cache Enable	
	0	Secondary Cache Disabled
	1	Secondary Cache Enabled
13:14	DrvOut: Output driver slew rate control	
	10	100% (fastest)
	11	83%
	00	67%
	01	50% (slowest)

Bit	Value	Mode Setting
15	Reserved: Must be zero	
16:17	Secondary cache size	
	0	512 KByte secondary cache
	1	1 MByte secondary cache
	2	2 MByte secondary cache
	3	Reserved
18:19	Reserved: Must be zero	
20	**Note**: Must be set to '1'	
21:32	Reserved: Must be zero	
33	**Note**: Must be set to '1'	
34:36	Reserved: Must be zero	
37	Reserved: Must be set to '1'	
38:288	Reserved: Must be zero	

Item #2 - Changes to SysAD[63:0] description

Issue: For all double-word accesses (read or write), the low-order 3 bits (SysAD[2:0]) will always be output as zero during the address phase.

Item #3 - Cache Error Exception

Issue: The following sentence has been added in Chapter 5, Cache Error Register (27) section and Cache Error Exception section: "If a read response (cached or uncached) is returned with bad parity, a cache error exception is taken."

Item #4 - Changed Description for Special Vector

Issue: In Chapter 5, Cache Error Exception section, changed BEV = 0 to BEV = 1 for vector 0xFFFF FFFF BFC0 0300.