



Integrated Device Technology, Inc.

**IDT79R4600™ and
IDT79R4700™
ORION RISCProcessor
Hardware User's Manual**

**Documentation
Errata
Version 2.0.1**

Supplemental Information

This Errata 2.0.1 supplements information contained in the following technical literature:

*IDT79R4600™ and IDT79R4700™ ORION RISC Processor Hardware
User's Manual, April 1995, Version 2.0.*

List of Errata Items

1. The information reference to Appendix G on page A-148 is incorrect.
2. The boot mode settings table on page 9-7 is changed to say that serial bit 25 (reserved) must be set to 1.

Errata Description

1. The user referral to Appendix G in the WAIT format section of Appendix A is incorrect. For a more detailed explanation of the WAIT format see Appendix D, "Standby Mode Operation," on page D-1 of the user's manual.
2. Table 9.2 on page 9-7 should be corrected to read as follows:

Serial Bit	Value	Mode Setting
19..24		Reserved (must be zero)
25		Reserved (must be one)
26..255		Reserved (must be zero)

Errata Revision History

Errata 2.0.0	3/12/96	First errata.
Errata 2.0.1	6/7/96	Added item 2.