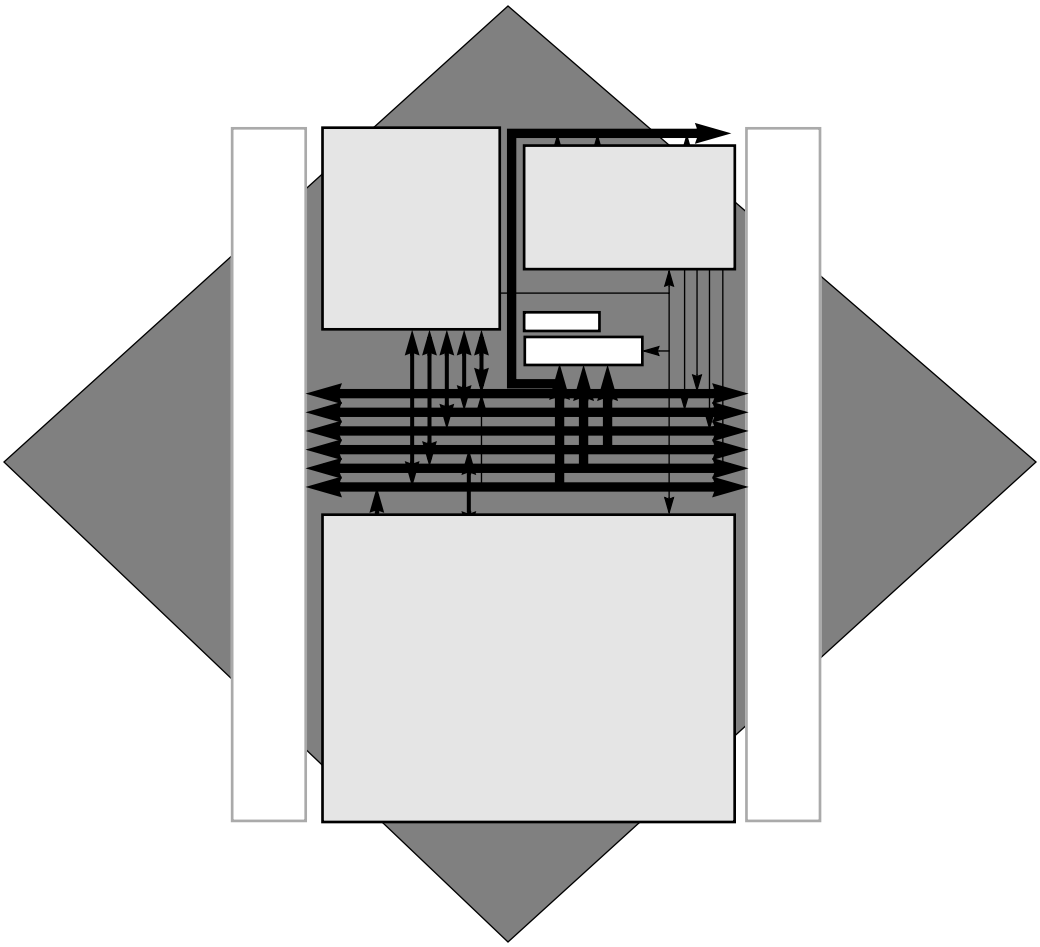
SECTION 2
DSP56K CENTRAL ARCHITECTURE OVERVIEW



SECTION CONTENTS

2.1 DSP56K CENTRAL ARCHITECTURE OVERVIEW

The DSP56K family of processors is built on a standard central processing module. In the expansion area around the central processing module, the chip can support various configurations of memory and peripheral modules which may change from family member to family member. This section introduces the architecture and the major components of the central processing module.

The central components are:

- Data Buses
- Address Buses
- Data Arithmetic Logic Unit (data ALU)
- Address Generation Unit (AGU)
- Program Control Unit (PCU)
- Memory Expansion (Port A)
- On-Chip Emulator (OnCE™) circuitry
- Phase-locked Loop (PLL) based clock circuitry

Figure 2-1 shows a block diagram of a typical DSP56K family processor, including the central processing module and a nonspecific expansion area for memory and peripherals. The following paragraphs give brief descriptions of each of the central components. Each of the components is explained in detail in subsequent chapters.

2.2 DATA BUSES

The DSP56K central processing module is organized around the registers of three independent execution units: the PCU, the AGU, and the data ALU. Data movement between the execution units occurs over four bidirectional 24-bit buses: the X data bus (XDB), the Y data bus (YDB), the program data bus (PDB), and the global data bus (GDB). (Certain instructions treat the X and Y data buses as one 48-bit data bus by concatenating them.) Data transfers between the data ALU and the X data memory or Y data memory occur over XDB and YDB, respectively. XDB and YDB are kept local on the chip to maximize speed and minimize power dissipation. All other data transfers, such as I/O transfers with peripherals, occur over the GDB. Instruction word prefetches occur in parallel over the PDB.

The bus structure supports general register-to-register, register-to-memory, and memory-to-register data movement. It can transfer up to two 24-bit words and one 56-bit word in the same instruction cycle. Transfers between buses occur in the internal bus switch.

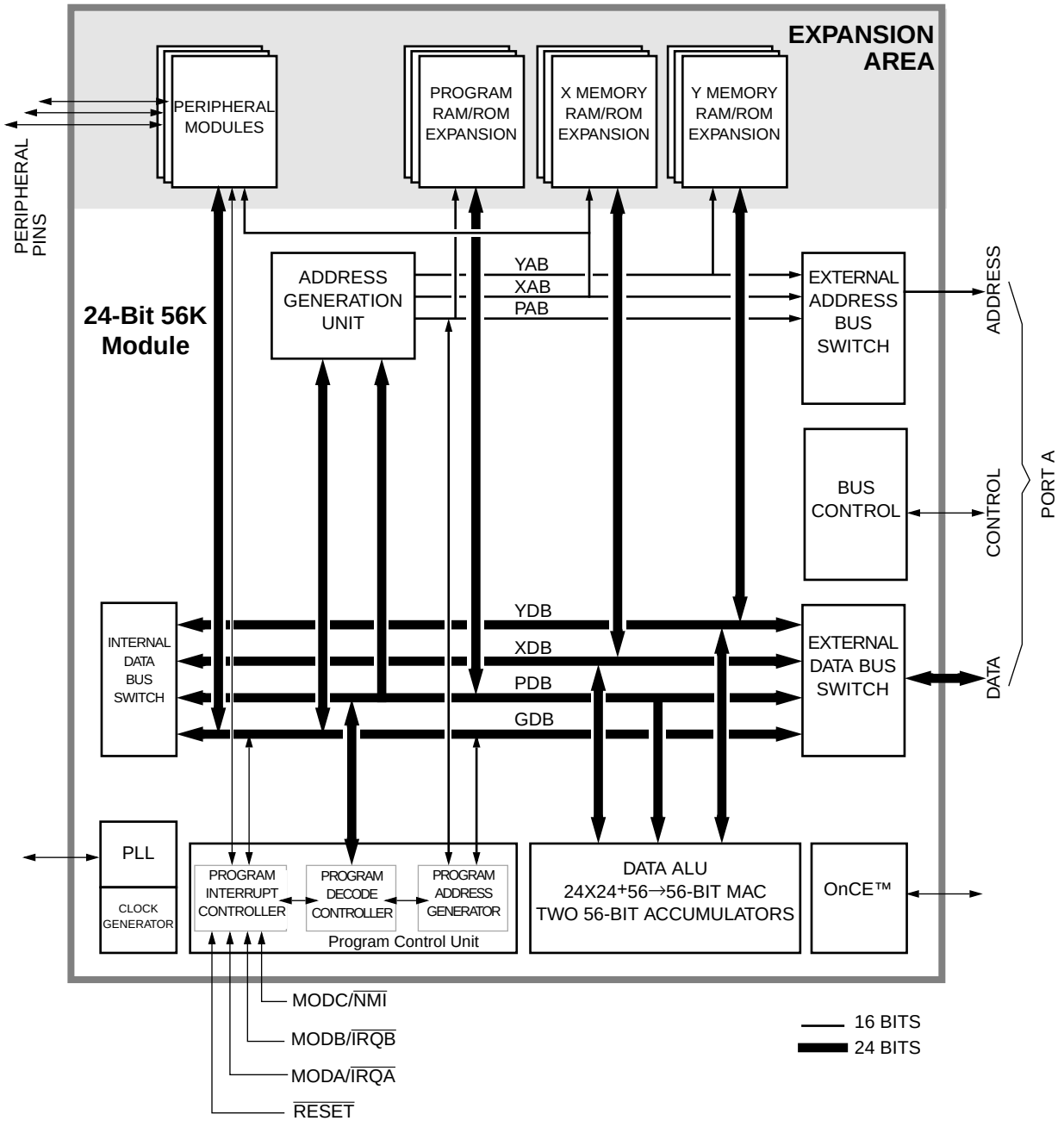


Figure 2-1 DSP56K Block Diagram

2.3 ADDRESS BUSES

Addresses are specified for internal X data memory and Y data memory on two unidirectional 16-bit buses — X address bus (XAB) and Y address bus (YAB). Program memory addresses are specified on the bidirectional program address bus (PAB). External mem-

ory spaces are addressed over a single 16-bit unidirectional address bus driven by a three-input multiplexer that can select the XAB, the YAB, or the PAB. Only one external memory access can be made in an instruction cycle. There is no speed penalty if only one external memory space is accessed in an instruction cycle. However, if two or three external memory spaces are accessed in a single instruction, there will be a one or two instruction cycle execution delay, respectively.

A bus arbitrator controls external access.

2.3.1 Internal Bus Switch

Transfers between buses occur in the internal bus switch. The internal bus switch, which is similar to a switch matrix, can connect any two internal buses without adding any pipeline delays. This flexibility simplifies programming.

2.3.2 Bit Manipulation Unit

The bit manipulation unit is physically located in the internal bus switch block because the internal data bus switch can access each memory space. The bit manipulation unit performs bit manipulation operations on memory locations, address registers, control registers, and data registers over the XDB, YDB, and GDB.

2.4 DATA ALU

The data ALU performs all of the arithmetic and logical operations on data operands. It consists of four 24-bit input registers, two 48-bit accumulator registers, two 8-bit accumulator extension registers, an accumulator shifter, two data bus shifter/limiter circuits, and a parallel, single-cycle, nonpipelined Multiply-Accumulator (MAC) unit.

2.5 ADDRESS GENERATION UNIT

The AGU performs all of the address storage and address calculations necessary to indirectly address data operands in memory. It operates in parallel with other chip resources to minimize address generation overhead. The AGU has two identical address arithmetic units that can generate two 16-bit addresses every instruction cycle. Each of the arithmetic units can perform three types of arithmetic: linear, modulo, and reverse-carry.

2.6 PROGRAM CONTROL UNIT

The program control unit performs instruction prefetch, instruction decoding, hardware DO loop control, and interrupt (or exception) processing. It consists of three components: the program address generator, the program decode controller, and the program interrupt controller. It contains a 15-level by 32-bit system stack memory and the following six di-

rectly addressable registers: the program counter (PC), loop address (LA), loop counter (LC), status register (SR), operating mode register (OMR), and stack pointer (SP). The 16-bit PC can address 65,536 locations in program memory space.

There are four mode and interrupt control pins that provide input to the program interrupt controller. The Mode Select A/External Interrupt Request A(MODA/$\overline{\text{IRQA}}$) and Mode Select B/External Interrupt Request B (MODB/$\overline{\text{IRQB}}$) pins select the chip operating mode and receive interrupt requests from external sources.

The Mode Select C/Non-Maskable Interrupt (MODC/$\overline{\text{NMI}}$) pin provides further operating mode options and non-maskable interrupt input.

The RESET pin resets the chip. When it is asserted, it initializes the chip and places it in the reset state. When it is deasserted, the chip assumes the operating mode indicated by the MODA, MODB, and MODC pins.

2.7 MEMORY EXPANSION PORT (PORT A)

Port A synchronously interfaces with a wide variety of memory and peripheral devices over a common 24-bit data bus. These devices include high-speed static RAMs, slower memory devices, and other DSPs and MPUs in master/slave configurations. This variety is possible because the expansion bus timing is programmable and can be tailored to match the speed requirements of the different memory spaces. Not all DSP56K family members feature a memory expansion port. See the individual device's User's Manual to determine if a particular chip includes this feature.

2.8 ON-CHIP EMULATOR (OnCE)

DSP56K on-chip emulation (OnCE) circuitry allows the user to interact with the DSP56K and its peripherals non-intrusively to examine registers, memory, or on-chip peripherals. It provides simple, inexpensive, and speed independent access to the internal registers for sophisticated debugging and economical system development.

Dedicated OnCE pins allow the user to insert the DSP into its target system and retain debug control without sacrificing other user accessible on-chip resources. The design eliminates the costly cabling and the access to processor pins required by traditional emulator systems.

2.9 PHASE-LOCKED LOOP (PLL) BASED CLOCKING

The PLL allows the DSP to use almost any available external system clock for full-speed operation, while also supplying an output clock synchronized to a synthesized internal clock. The PLL performs frequency multiplication, skew elimination, and low-power division.