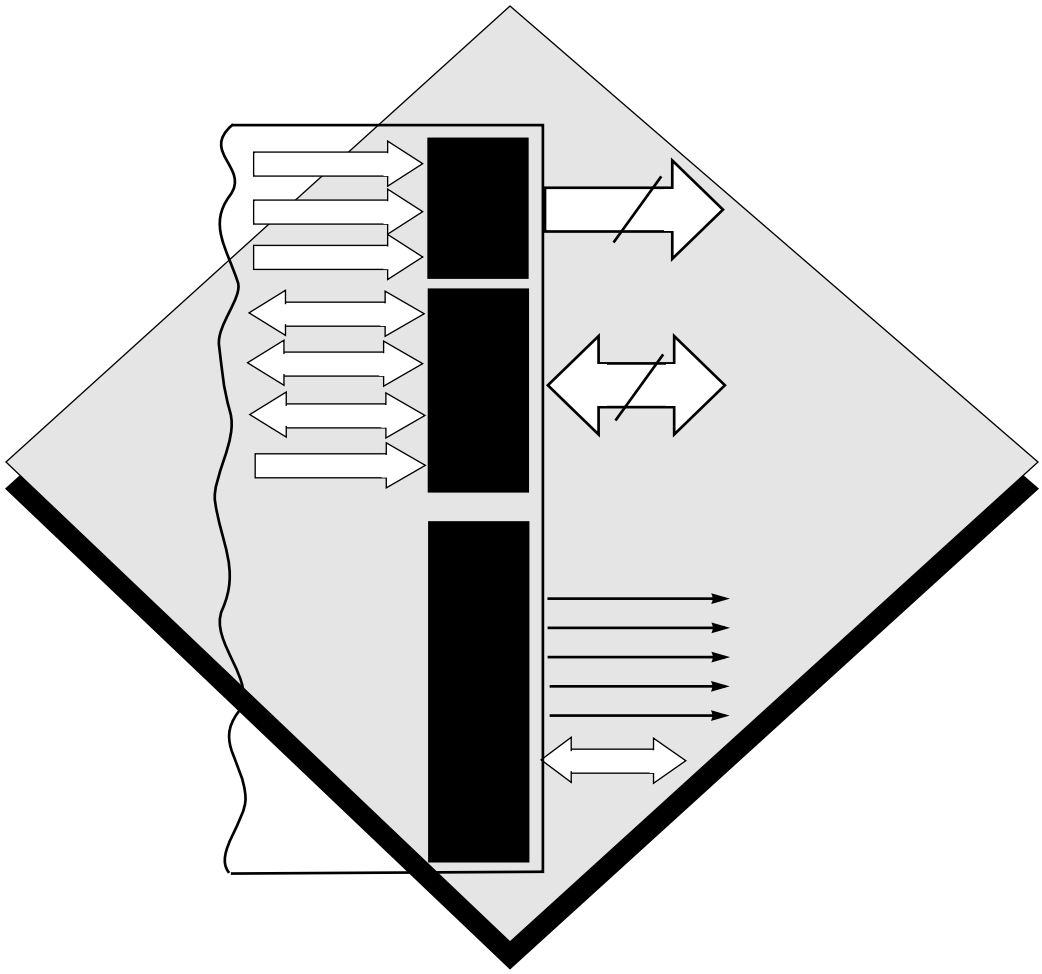
SECTION 8
PORT A



SECTION CONTENTS

8.1 PORT A OVERVIEW

Port A provides a versatile interface to external memory, allowing economical connection with fast memories, slow memories/devices, and multiple bus master systems. This section introduces the signals associated with this memory expansion port that are common among the members of the DSP56K family of processors which feature Port A. Certain characteristics, such as signaling, timing, and bus arbitration, vary between members of the processor family and are detailed in each device's own User's Manual.

Port A has two power-reduction features. It can access internal memory spaces, toggling only the external memory signals that need to change, and eliminate unneeded switching current. Also, if conditions allow the processor to operate at a lower memory speed, wait states can be added to the external memory access to significantly reduce power while the processor accesses those memories.

8.2 PORT A INTERFACE

The DSP56K processor can access one or more of its memory sources (X data memory, Y data memory, and program memory) while it executes an instruction. The memory sources may be either internal or external to the DSP. Three address buses (XAB, YAB, and PAB) and four data buses (XDB, YDB, PDB, and GDB) are available for internal memory accesses during one instruction cycle. Port A's one address bus and one data bus are available for external memory accesses. If all memory sources are internal to the DSP, one or more of the three memory sources may be accessed in one instruction cycle (i.e., program memory access or program memory access plus an X, Y, XY, or L memory reference). However, when one or more of the memories are external to the chip, memory references may require additional instruction cycles because only one external memory access can occur per instruction cycle.

If an instruction cycle requires more than one external access, the processor will make the accesses in the following priority: X memory, Y memory, and program memory. It takes one instruction cycle for each external memory access – i.e., one access can be executed in one instruction cycle, two accesses take two instruction cycles, etc. Since the external bus is only 24 bits wide, one XY or long external access will take two instruction cycles.

The port A external data bus shown in Figure 8-1 is 24 bits wide. The 16-bit address bus can sustain a rate of one memory access per instruction cycle (using no-wait-state memory which is discussed in Section 8.2.5.)

Figure 8-1 shows the port A signals divided into their three functional groups: address bus

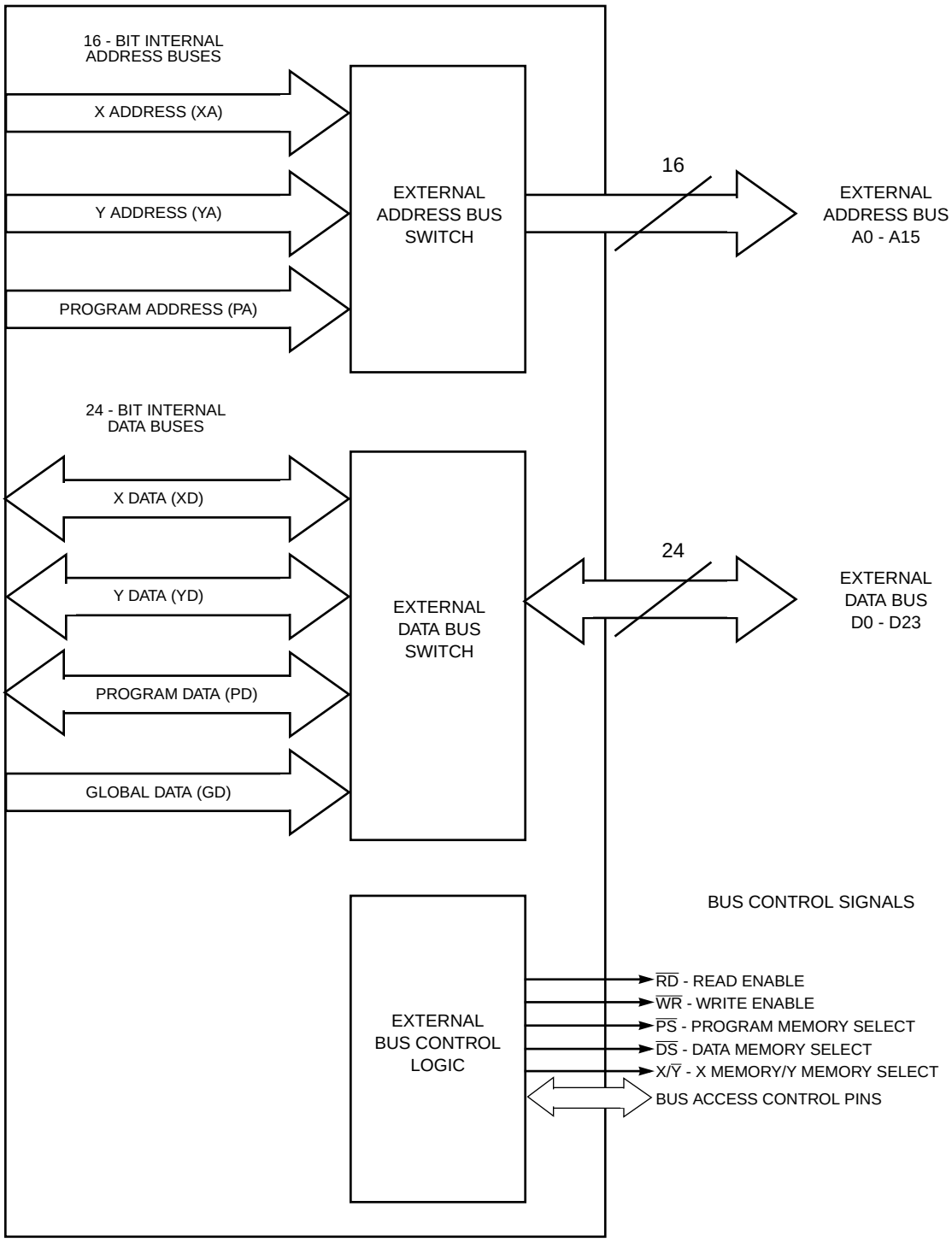


Figure 8-1 Port A Signals

signals (A0-A15), data bus signals (D0-D15), and bus control. The bus control signals can

be subdivided into three additional groups: read/write control ($\overline{RD}$ and $\overline{WR}$), address space selection (including program memory select ($\overline{PS}$), data memory select ($\overline{DS}$), and X/$\overline{Y}$ select) and bus access control.

The read/write controls are self-descriptive. They can be used as decoded read and write controls, or, the write signal can be used as the read/write control and the read signal can be used as an output enable (or data enable) control for the memory. Decoding in this fashion simplifies the connection to high-speed random-access memories (RAMs). The address space selection signals can be considered as additional address signals, which extend the addressable memory from 64K words to 192K words

Note: Depending on system design, unused inputs should have pullup resistors for two reasons: 1) floating inputs draw excessive power, and 2) a floating input can cause erroneous operation. For example, during RESET, all signals are three-stated. Output pins $\overline{PS}$ and $\overline{DS}$ may require pullup resistors because, without them, the signals may become active and may cause two or more memory chips to try to simultaneously drive the external data bus, which can damage the memory chips. A pullup resistor in the 50K-ohm range should be sufficient.

8.2.1 Read/Write Control Signals

The following paragraphs describe the Port A read/write control signals. These pins are three-stated during reset and may require pullup resistors to prevent erroneous operation of a memory device or other external components.

8.2.1.1 Program Memory Select ($\overline{PS}$)

This three-state output is asserted only when external program memory is referenced.

8.2.1.2 Data Memory Select ($\overline{DS}$)

This three-state output is asserted only when external data memory is referenced.

8.2.1.3 X/$\overline{Y}$ Select (X/$\overline{Y}$)

This three-state output selects which external data memory space (X or Y) is referenced by $\overline{DS}$.

8.2.2 Port A Address and Data Bus Signals

The following paragraphs describe the Port A address and data bus signals. These pins are three-stated during reset and may require pullup resistors to prevent erroneous operation.

8.2.2.1 Address (A0–A15)

These three-state output pins specify the address for external program and data memory accesses. To minimize power dissipation, A0–A15 do not change state when external memory spaces are not being accessed.

8.2.2.2 Data (D0–D23)

These pins provide the bidirectional data bus for external program and data memory accesses. D0–D23 are in the high-impedance state when the bus grant signal is asserted.

8.2.3 Port A Bus Control Signals

The following paragraphs describe the Port A bus control signals. The bus control signals provide the means to connect additional bus masters (which may be additional DSPs, microprocessors, direct memory access (DMA) controllers, etc.) to the port A bus. They are three-stated during reset and may require pullup resistors to prevent erroneous operation.

8.2.3.1 Read Enable ($\overline{RD}$)

This three-state output is asserted to read external memory on the data bus (D0–D23).

8.2.3.2 Write Enable ($\overline{WR}$)

This three-state output is asserted to write external memory on the data bus (D0–D23).

8.2.3.3 Port A Access Control Signals

Port A features a group of configurable pins that perform bus arbitration and bus access control. The pins, such as Bus Needed ($\overline{BN}$), Bus Request. ($\overline{BR}$), Bus Grant ($\overline{BG}$), Bus Wait ($\overline{WT}$), and Bus Strobe ($\overline{BS}$), and their designations differ between members of the DSP56K family and are explained in the respective devices' user manuals.

8.2.4 Interrupt and Mode Control

Port A features a pin set that selects the chip's operating mode and receives interrupt requests from external sources. The pins and their designations vary between members of the DSP56K family and are explained in the respective devices' user manuals.

8.2.5 Port A Wait States

The DSP56K processor features two methods to allow the user to accommodate slow memory by changing the port A bus timing. The first method uses the16-bit bus control register (BCR), which resides in X Data memory space. The BCR allows a fixed number of wait states to be inserted in a given memory access to all locations in any one of the four memory spaces: X, Y, P, and I/O. The second method uses the bus strobe/wait ($\overline{BS}$/

$\overline{WT}$) facility, which allows an external device to insert an arbitrary number of wait states when accessing either a single location or multiple locations of external memory or I/O space. Wait states are executed until the external device releases the DSP to finish the external memory cycle. An internal wait-state generator can be programmed using the BCR to insert up to15 wait states if it is known ahead of time that access to slower memory or I/O devices is required. A bus wait signal allows an external device to control the number of wait states (not limited to 15) inserted in a bus access operation.