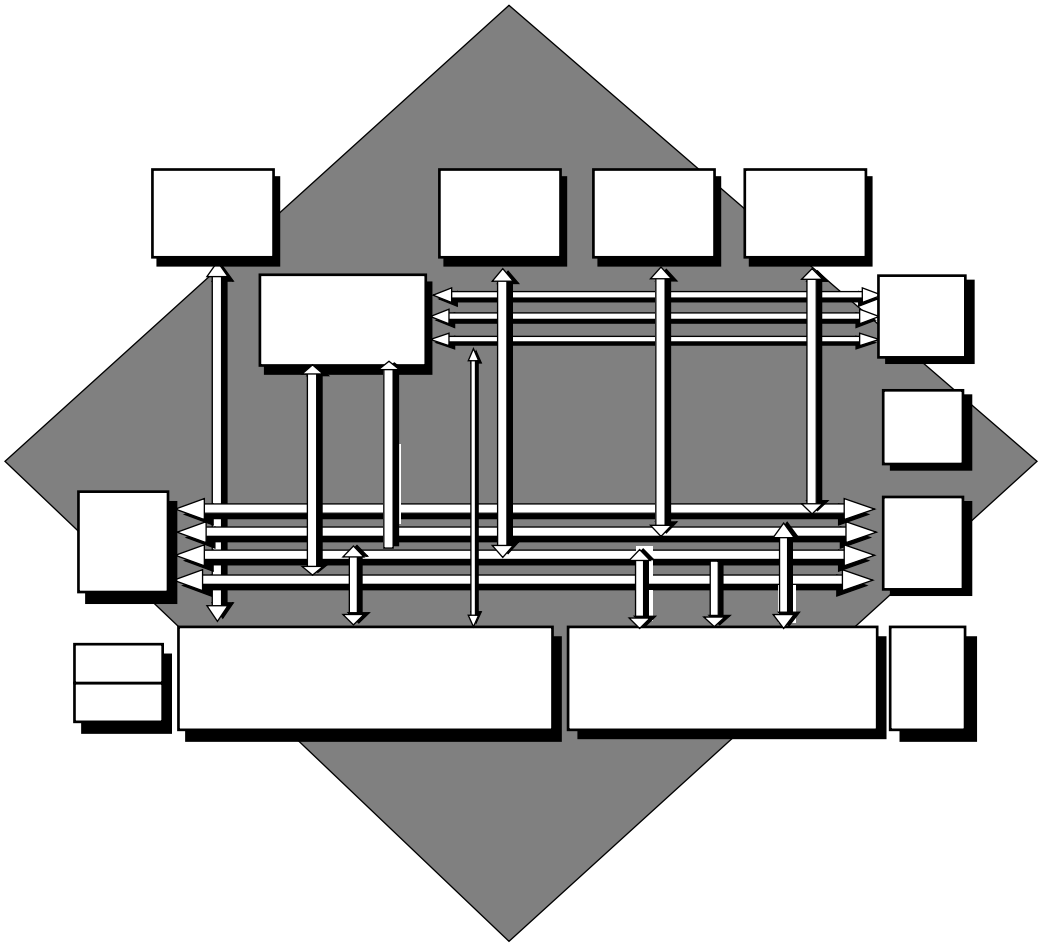
SECTION 1
DSP56K FAMILY INTRODUCTION



SECTION CONTENTS

1.1 INTRODUCTION

The DSP56K Family is Motorola's series of 24-bit general purpose Digital Signal Processors (DSPs*). The family architecture features a central processing module that is common to the various family members, such as the DSP56002 and the DSP56004.

Note: The DSP56000 and the DSP56001 are not based on the central processing module architecture and should not be used with this manual. They will continue to be described in the DSP56000/DSP56001 User's Manual (DSP56000UM/AD Rev. 2).

This manual describes the DSP56K Family's central processor and instruction set. It is intended to be used with a family member's User's Manual, such as the DSP56002 User's Manual.

The User's Manual presents the device's specifics, including pin descriptions, operating modes, and peripherals. Packaging and timing information can be found in the device's Technical Data Sheet.

This chapter introduces general DSP theory and discusses the features and benefits of the Motorola DSP56K family of 24-bit processors. It also presents a brief description of each of the sections of the manual.

1.2 ORIGIN OF DIGITAL SIGNAL PROCESSING

DSP is the arithmetic processing of real-time signals sampled at regular intervals and digitized. Examples of DSP processing include the following:

- Filtering of signals
- Convolution, which is the mixing of two signals
- Correlation, which is a comparison of two signals
- Rectification, amplification, and/or transformation of a signal

All of these functions have traditionally been performed using analog circuits. Only recently has semiconductor technology provided the processing power necessary to digitally perform these and other functions using DSPs.

Figure 1-1 shows a description of analog signal processing. The circuit in the illustration filters a signal from a sensor using an operational amplifier, and controls an actuator with the result. Since the ideal filter is impossible to design, the engineer must design the filter for acceptable response, considering variations in temperature, component aging, power supply variation, and component accuracy. The resulting circuit typically has low noise immunity, requires adjustments, and is difficult to modify.

*This manual uses the acronym DSP for Digital Signal Processing or Digital Signal Processor, depending on the context.

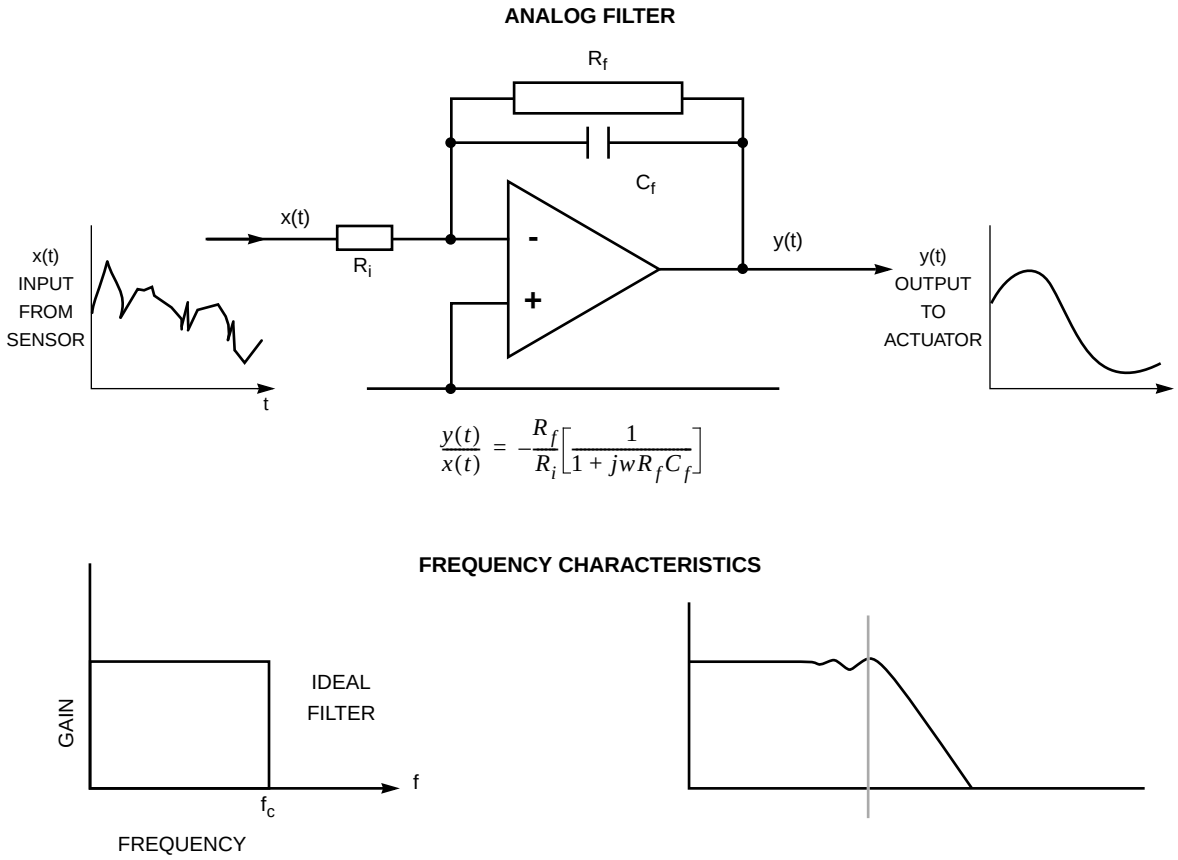


Figure 1-1 Analog Signal Processing

The equivalent circuit using a DSP is shown in Figure 1-2. This application requires an analog-to-digital (A/D) converter and digital-to-analog (D/A) converter in addition to the DSP. Even with these additional parts, the component count can be lower using a DSP due to the high integration available with current components.

Processing in this circuit begins by band-limiting the input with an anti-alias filter, eliminating out-of-band signals that can be aliased back into the pass band due to the sampling process. The signal is then sampled, digitized with an A/D converter, and sent to the DSP.

The filter implemented by the DSP is strictly a matter of software. The DSP can directly implement any filter that can also be implemented using analog techniques. Also, adaptive filters can be easily implemented using DSP, whereas these filters are extremely difficult to implement using analog techniques.

The DSP output is processed by a D/A converter and is low-pass filtered to remove the effects of digitizing. In summary, the advantages of using the DSP include the following:

- Fewer components
- Stable, deterministic performance
- Wide range of applications
- High noise immunity and power-supply rejection
- Self-test can be built in
- No filter adjustments
- Filters with much closer tolerances
- Adaptive filters easily implemented

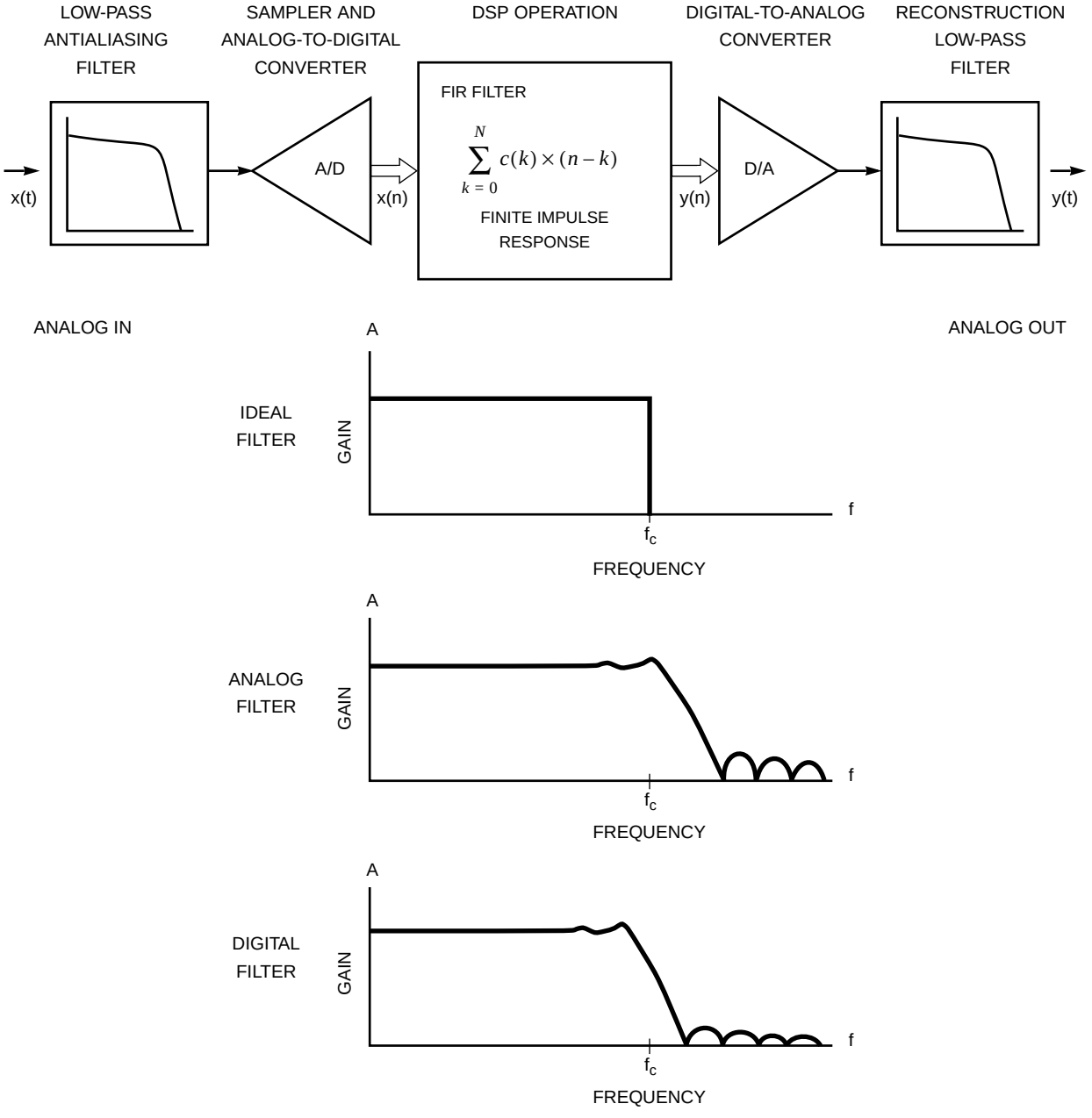


Figure 1-2 Digital Signal Processing

The DSP56K family is not designed for a particular application but is designed to execute commonly used DSP benchmarks in a minimum time for a single-multiplier architecture. For example, a cascaded, 2nd-order, four-coefficient infinite impulse response (IIR) biquad section has four multiplies for each section. For that algorithm, the theoretical minimum number of operations for a single-multiplier architecture is four per section. Table 1-1 shows a list of benchmarks with the number of instruction cycles a DSP56K chip uses compared to the number of multiplies the algorithm requires.

Table 1-1 Benchmark Summary in Instruction Cycles

Benchmark	Number of Cycles	Number of Algorithm Multiplies
Real Multiply	3	1
N Real Multiplies	2N	N
Real Update	4	1
N Real Updates	2N	N
N Term Real Convolution (FIR)	N	N
N Term Real * Complex Convolution	2N	N
Complex Multiply	6	4
N Complex Multiplies	4N	N
Complex Update	7	4
N Complex Updates	4N	4N
N Term Complex Convolution (FIR)	4N	4N
N^{th} - Order Power Series	2N	2N
2^{nd} - Order Real Biquad Filter	7	4
N Cascaded 2^{nd} - Order Biquads	4N	4N
N Radix Two FFT Butterflies	6N	4N

These benchmarks and others are used independently or in combination to implement functions whose characteristics are controlled by the coefficients of the benchmarks being executed. Useful functions using these and other benchmarks include the following:

Digital Filtering
- Finite Impulse Response (FIR)
- Infinite Impulse Response (IIR)
- Matched Filters (Correlators)
- Hilbert Transforms
- Windowing
- Adaptive Filters/Equalizers

Signal Processing
- Compression (e.g., Linear Predictive Coding of Speech Signals)
- Expansion
- Averaging
- Energy Calculations
- Homomorphic Processing
- Mu-law/A-law to/from Linear Data Conversion

Data Processing
- Encryption/Scrambling
- Encoding (e.g., Trellis Coding)
- Decoding (e.g., Viterbi Decoding)

Numeric Processing
- Scaler, Vector, and Matrix Arithmetic
- Transcendental Function Computation (e.g., Sin(X), Exp(X))
- Other Nonlinear Functions
- Pseudo-Random-Number Generation

Modulation
- Amplitude
- Frequency
- Phase

Spectral Analysis
- Fast Fourier Transform (FFT)
- Discrete Fourier Transform (DFT)
- Sine/Cosine Transforms
- Moving Average (MA) Modeling
- Autoregressive (AR) Modeling
- ARMA Modeling

Useful applications are based on combining these and other functions. DSP applications affect almost every area in electronics because any application for analog electronic circuitry can be duplicated using DSP. The advantages in doing so are becoming more compelling as DSPs become faster and more cost effective.Some typical applications for DSPs are presented in the following list:

Telecommunication
- Tone Generation
- Dual-Tone Multifrequency (DTMF)
- Subscriber Line Interface
- Full-Duplex Speakerphone
- Teleconferencing
- Voice Mail
- Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder
- Medium-Rate Vocoders
- Noise Cancelation
- Repeaters
- Integrated Services Digital Network (ISDN) Transceivers
- Secure Telephones

Data Communication
- High-Speed Modems
- Multiple Bit-Rate Modems
- High-Speed Facsimile

Radio Communication
- Secure Communications
- Point-to-Point Communications
- Broadcast Communications
- Cellular Mobile Telephone

Computer
- Array Processors
- Work Stations
- Personal Computers
- Graphics Accelerators

Image Processing
Pattern Recognition
Optical Character Recognition
Image Restoration
Image Compression
Image Enhancement
Robot Vision

Graphics
3-D Rendering
Computer-Aided Engineering (CAE)
Desktop Publishing
Animation

Instrumentation
Spectral Analysis
Waveform Generation
Transient Analysis
Data Acquisition

Speech Processing
Speech Synthesizer
Speech Recognizer
Voice Mail
Vocoder
Speaker Authentication
Speaker Verification

Audio Signal Processing
Digital AM/FM Radio
Digital Hi-Fi Preamplifier
Noise Cancelation
Music Synthesis
Music Processing
Acoustic Equalizer

High-Speed Control
Laser-Printer Servo
Hard-Disk Servo
Robotics
Motor Controller
Position and Rate Controller

Vibration Analysis
Electric Motors
Jet Engines
Turbines

Medical Electronics
Cat Scanners
Sonographs
X-Ray Analysis
Electrocardiogram
Electroencephalogram
Nuclear Magnetic Resonance Analysis

Digital Video
Digital Television
High-Resolution Monitors

Radar and Sonar Processing
Navigation
Oceanography
Automatic Vehicle Location
Search and Tracking

Seismic Processing
Oil Exploration
Geological Exploration

As shown in Figure 1-3, the keys to DSP are as follows:

- The Multiply/Accumulate (MAC) operation
- Fetching operands for the MAC
- Program control to provide versatile operation
- Input/Output to move data in and out of the DSP

MAC is the basic operation used in DSP. The DSP56K family of processors has a dual Harvard architecture optimized for MAC operations. Figure 1-3 shows how the DSP56K

architecture matches the shape of the MAC operation. The two operands, C() and X(), are directed to a multiply operation, and the result is summed. This process is built into the chip by using two separate memories (X and Y) to feed a single-cycle MAC. The entire process must occur under program control to direct the correct operands to the multiplier and save the accumulator as needed. Since the two memories and the MAC are independent, the DSP can perform two moves, a multiply and an accumulate, in a single operation. As a result, many of the benchmarks shown in Table 1-1 can be executed at or near the theoretical maximum speed for a single-multiplier architecture.

1.3 SUMMARY OF DSP56K FAMILY FEATURES

The high throughput of the DSP56K family of processors makes them well suited for communication, high-speed control, numeric processing and computer and audio applications. The main features that contribute to this high throughput include:

- **Speed** — Speeds high enough to easily address applications traditionally served by low-end floating point DSPs.

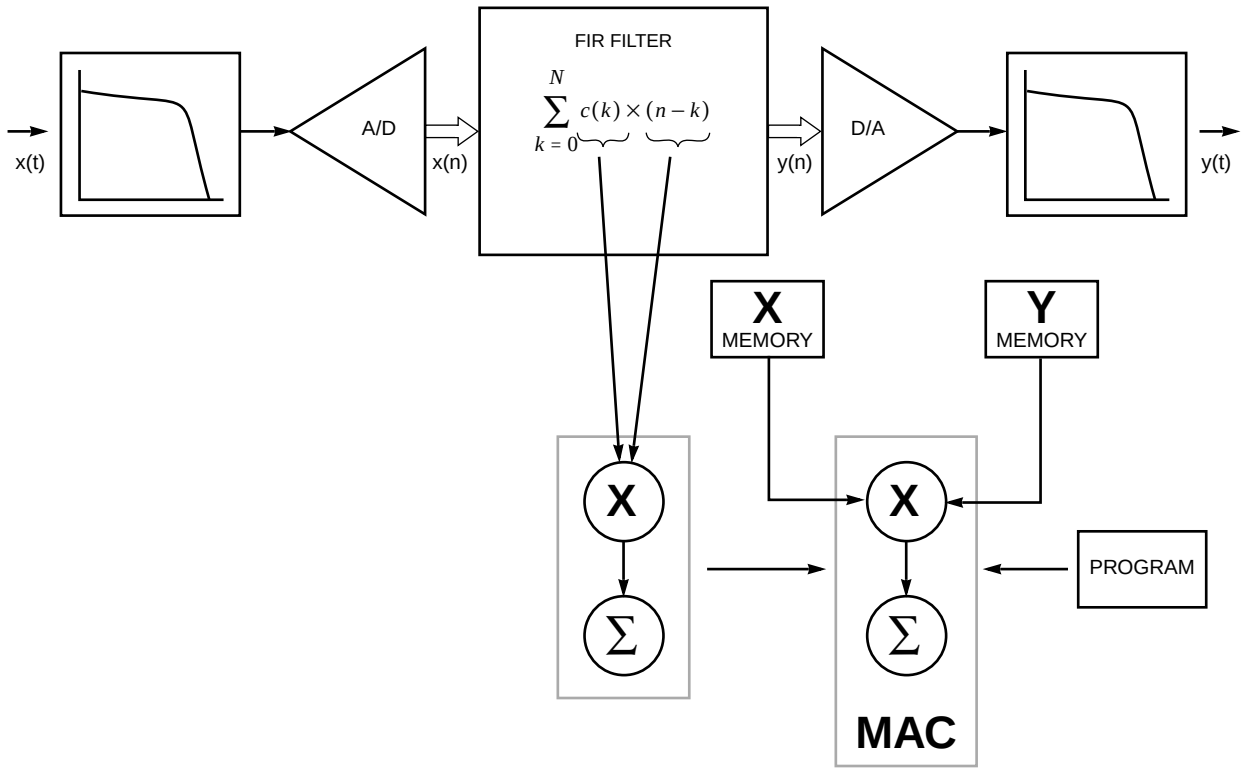


Figure 1-3 DSP Hardware Origins

- **Precision** — The data paths are 24 bits wide, providing 144 dB of dynamic range; intermediate results held in the 56-bit accumulators can range over 336 dB.
- **Parallelism** — Each on-chip execution unit (AGU, program control unit, data ALU), memory, and peripheral operates independently and in parallel with the other units through a sophisticated bus system. The data ALU, AGU, and program control unit operate in parallel so that an instruction prefetch, a 24-bit x 24-bit multiplication, a 56-bit addition, two data moves, and two address-pointer updates using one of three types of arithmetic (linear, modulo, or reverse-carry) can be executed in a single instruction cycle. This parallelism allows a four-coefficient IIR filter section to be executed in only four cycles, the theoretical minimum for single-multiplier architecture. At the same time, the two serial controllers can send and receive full-duplex data, and the host port can send/receive simplex data.
- **Flexibility** — While many other DSPs need external communications circuitry to interface with peripheral circuits (such as A/D converters, D/A converters, or host processors), the DSP56K family provides on-chip serial and parallel interfaces which can support various configurations of memory and peripheral modules
- **Sophisticated Debugging**— Motorola's on-chip emulation technology (OnCE) allows simple, inexpensive, and speed independent access to the internal registers for debugging. OnCE tells application programmers exactly what the status is within the registers, memory locations, buses, and even the last five instructions that were executed.
- **Phase-locked Loop (PLL) Based Clocking** — PLL allows the chip to use almost any available external system clock for full-speed operation while also supplying an output clock synchronized to a synthesized internal core clock. It improves the synchronous timing of the processors' external memory port, eliminating the timing skew common on other processors.
- **Invisible Pipeline** — The three-stage instruction pipeline is essentially invisible to the programmer, allowing straightforward program development in either assembly language or a high-level language such as a full Kernighan and Ritchie C.
- **Instruction Set** — The instruction mnemonics are MCU-like, making the transition from programming microprocessors to programming the chip as easy as possible. The orthogonal syntax controls the parallel execution units. The hardware DO loop instruction and the repeat (REP) instruction make writing straight-line code obsolete.

- **DSP56001 Compatibility** — All members of the DSP56K family are downward compatible with the DSP56001, and also have added flexibility, speed, and functionality.
- **Low Power** — As a CMOS part, the DSP56000/DSP56001 is inherently very low power and the STOP and WAIT instructions further reduce power requirements.

1.4 MANUAL ORGANIZATION

This manual describes the central processing module of the DSP56K family in detail and provides practical information to help the user:

- Understand the operation of the DSP56K family
- Design parallel communication links
- Design serial communication links
- Code DSP algorithms
- Code communication routines
- Code data manipulation algorithms
- Locate additional support

The following list describes the contents of each section and each appendix:

Section 2 – DSP56K Central Architecture Overview

The DSP56K central architecture consists of the data arithmetic logic unit (ALU), address generation unit (AGU), program control unit, On-Chip Emulation (OnCE) circuitry, the phase locked loop (PLL) based clock oscillator, and an external memory port (Port A). This section describes each subsystem and the buses interconnecting the major components in the DSP56K central processing module.

Section 3 – Data Arithmetic Logic Unit

This section describes in detail the data ALU and its programming model.

Section 4 – Address Generation Unit

This section specifically describes the AGU, its programming model, address indirect modes, and address modifiers.

Section 5 – Program Control Unit

This section describes in detail the program control unit and its programming model.

Section 6 – Instruction Set Introduction

This section presents a brief description of the syntax, instruction formats, operand/memory references, data organization, addressing modes, and instruction set. A detailed description of each instruction is given in APPENDIX A - INSTRUCTION SET DETAILS.

Section 7 – Processing States

This section describes the five processing states (normal, exception, reset, wait, and stop).

Section 8 – Port A

This section describes the external memory port, its control register, and control signals.

Section 9 – PLL Clock Oscillator

This section describes the PLL and its functions

Section 10 – On-Chip Emulator (OnCE)

This section describes the OnCE circuitry and its functions.

Section 11 – Additional Support

This section presents a brief description of current support products and services and information on where to obtain them.

Appendix A – Instruction Set Details

A detailed description of each DSP56K family instruction, its use, and its affect on the processor are presented.

Appendix B – Benchmarks

DSP5K family benchmark results are listed in this appendix.