Intel® IA-64 Architecture Software Developer's Manual

Specification Update

Revision 2.0

October 2000

Notice: IA-64 processors may contain design defects or errors known as errata which may cause the product to deviate from published specifications.

Document Number: 248699-002

Contents

Revision History

Date	Revision	Description
April 2000	1.0	Initial version of this document.
October 2000	2.0	Addded changes to performance monitoring section (section 7.8, volume IV) Added a clarification to class pr-writers-int in Table A-5 of Volume 2 Added a clarification to section 4.4.6.1 of Volume 2

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents in the table below. This document is a compilation of specification changes, specification clarifications and document changes. It does not cover errata.

Affected Documents/Related Documents

Title	Order #
IA-64 Architecture Software Developer's Manual, Volume 1: IA-64 Application Architecture	245317-002
IA-64 Architecture Software Developer's Manual, Volume 2: IA-64 System Architecture	245318-002
IA-64 Architecture Software Developer's Manual, Volume 3: Instruction Set Reference; and Volume 4: Itanium™ Processor Programmer's Guide	245319-002

Nomenclature

Specification Changes are modifications to the current published specifications for the Itanium processor. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the IA-64 Architecture SDM.

Summary Table of Changes

The following tables indicate the specification changes, specification clarifications, or documentation changes which apply to the *Intel® IA-64 Architecture Software Developer's Manual*.

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Specification Changes

Volume	No.	Page	Section	SPECIFICATION CHANGES
II	1		7.8	Performance monitor events qualification changes
IV	2		7.8	Changes in section 7.8: IA64_TAGGED_INST_RETIRED PREDICATE_SQUASHED_RETIRED UC_LOADS_RETIRED UC_STORES_RETIRED

Specification Clarifications

Volume.	No.	Page	Section	SPECIFICATION CLARIFICATIONS
II	1	A-22		Table A-5 class pr-writers-int
II	2	4-32		section 4.4.6.1 disabling prefetch and removing cacheability changes
IV	3		7.8	Changes in: section 6.2.8.2 IA-64 Branch Trace Buffer Reading BRANCH_EVENT BRANCH_TAKEN_SLOT

Documentation Changes

Volume.	No.	Page	Section	DOCUMENTATION CHANGES
IV	1		7.8	Changes in section 7.8: BRANCH_PREDICTOR.2nd_STAGE.ALL_PREDICTIONS

Specification Changes

1. Volume IV: section 7.8, Performance monitoring events qualification changes

In Chapter 7, section 7.8, Performance Monitor Event List, the event qualification for the following events should be updated as shown in the table below: (NOTE: Yes-Means qualification by item in column is possible, No-Means qualification by item in column is not possible)

Event	Instruction Address Range	Opcode Matching	Data Address Range
DATA_EAR_EVENTS			No
DTLB_MISSES			No
DTLB_INSERTS_HPW			No
DTC_MISSES			No
L1D_READS_RETIRED			Yes
L2_FLUSHES	Yes		
L2_MISSES		No	No
L2_REFERENCES		No	No
L3_REFERENCES	No	No	No

2. Volume IV: section 7.8, performing monitoring events definition changes

-P. 7-32, under IA64_TAGGED_INST_RETIRED
change
“The settings of PMC9 do not affect other event monitors”
TO
“The settings of PMC9 do not affect other event monitors”
<start a new paragraph here>
“Also, note that umask 0011 is distinct in that it also counts, in addition to instructions matched by the appropriate opcode matcher, architecturally invisible RSE fills and spills when the parent instruction (such as an alloc or br.ret) causing them is matched by the combination in PMC8. Thus the difference in counts obtained between using PMC8 and PMC9 as opcode matchers is the amount of RSE activity”.

-P.7-46, under PREDICATE_SQUASHED_RETIRED,
Change
“The count includes predicated off nop instructions. Predicated branches are not counted.”
TO
“The count includes all predicated off nops except nop.b’s. Predicated off B-syllables (including nop.b) are not counted.

-P.7-47, under UC_LOADS_RETIRED,
change
“the number of retired cacheable loads.”
TO
“the number of retired uncacheable or write coalescing loads.”

-P.7-47, under UC_STORES_RETIRED,
change
“the number of retired uncacheable stores”
TO
“the number of retired uncacheable or write coalescing stores.”

Specification Clarifications

1. Volume II: Table A-5 class pr-writers-int

In Table A-5 on P. A-22, for the class pr-writers-int, add pr-and-writers and pr-or-writers to the Events/Instructions column.

2. Volume II: section 4.4.6.1 PAL_MC_DRAIN procedure only causes cache line writeback transactions to be forced onto the bus, and does not guarantee that they reached main memory

Change the last paragraph of section 4.4.6.1on Page 4-32 to:

To further guarantee that any cache lines containing addresses belonging to page [X] have been evicted from all caches in the coherence domain and *forced onto the bus*, software must perform a PAL_MC_DRAIN operation on all processors in the coherence domain (via the IPI mechanism) after executing the above sequence. Note that this operation does not ensure that the cache lines have been written back to memory.
(The words “written back to memory” have been changed, and a new sentence was added at the end.)

3. Volume IV: section 7.8, Performance monitor events definition clarifications:

- P. 6-30, section 6.2.8.2 “IA-64 Branch Trace Buffer Reading”
Change the second to the last line to:
“If the target instruction bundle *or the bundle following it*, itself, contains a qualified IA-64 branch, the branch trace buffer either records a single trace buffer entry.....”

-P. 7-15, under BRANCH_EVENT
change
“counts the number of branch events, including multiway branches”
TO
“counts the number of branch events, including multiway branches captured by the Branch Trace Buffer”

-P. 7-28, under BRANCH_TAKEN_SLOT
change
“... that there were no taken branches in the given bundle”
TO
“.... that there were no taken branches in the given branch bundle. Use this monitor behind the downstream opcode matcher, rather than IA64_TAGGED_INST_RETIRED, to count dynamic br.calls and br.rets.

Documentation Changes

1. Volume IV, section 7.8, performance monitoring events typo:

-P.7-25, under BRANCH_PREDICTOR.2nd_STAGE.ALL_PREDICTIONS

In the last 6 lines of the algorithm ,change

“else

monitor++

if (TAC Hit)

Read Target from TAC

else

Follow Sequential Path”

TO

“else

if (TAC Hit)

monitor++

Read Target from TAC

else

Follow Sequential Path”