256K x 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C256- 7	70ns	20ns	130ns
KM41C256- 8	80ns	20ns	150ns
KM41C256-10	100ns	25ns	180ns

- **Fast Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V ± 10% power supply**
- **256 cycles/4ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, PLCC or ZIP**

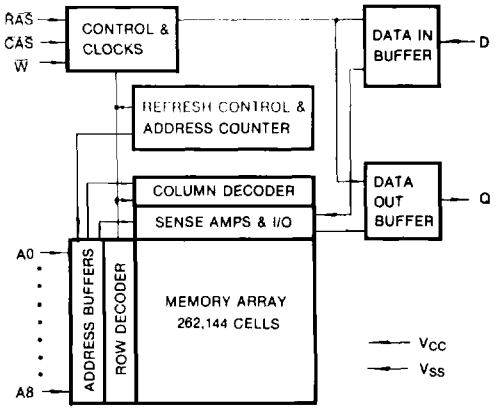
GENERAL DESCRIPTION

The Samsung KM41C256 is a CMOS high speed 262,144 bit x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

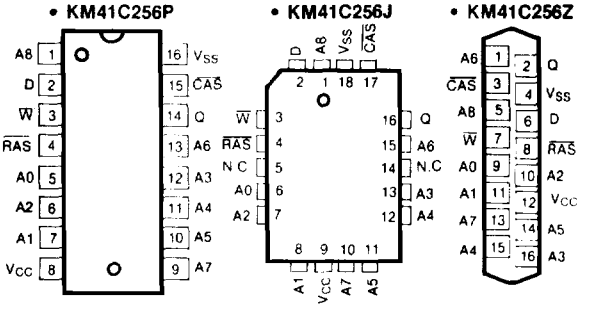
The KM41C256 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

The KM41C256 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A_0-A_8	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C256- 7	I_{CC1}	—	65	mA
	KM41C256- 8		—	55	mA
	KM41C256-10		—	45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C256- 7	I_{CC3}	—	65	mA
	KM41C256- 8		—	55	mA
	KM41C256-10		—	45	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C256- 7	I_{CC4}	—	40	mA
	KM41C256- 8		—	35	mA
	KM41C256-10		—	30	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C256- 7	I_{CC6}	—	65	mA
	KM41C256- 8		—	55	mA
	KM41C256-10		—	45	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0V \leq V_{IN} \leq 6.5V$, all other pins not under test = 0 volts.)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)	V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)	V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A = 25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_8)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C256-7		KM41C256-8		KM41C256-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	25	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	

AC CHARACTERISTICS (Continued)

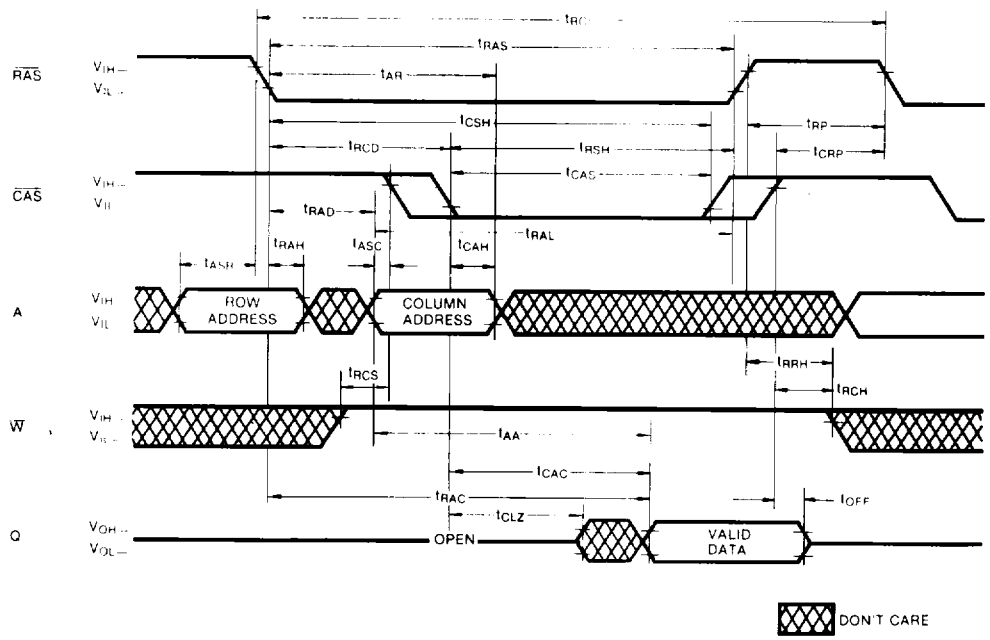
Standard Operation	Symbol	KM41C256-7		KM41C256-8		KM41C256-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh counter test $\overline{CAS}$ precharge	t_{CPT}	35		40		50		ns	
Fast Page mode cycle time	t_{PC}	45		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast page mode read-modify-write	t_{PRWC}	70		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures the t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} < t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

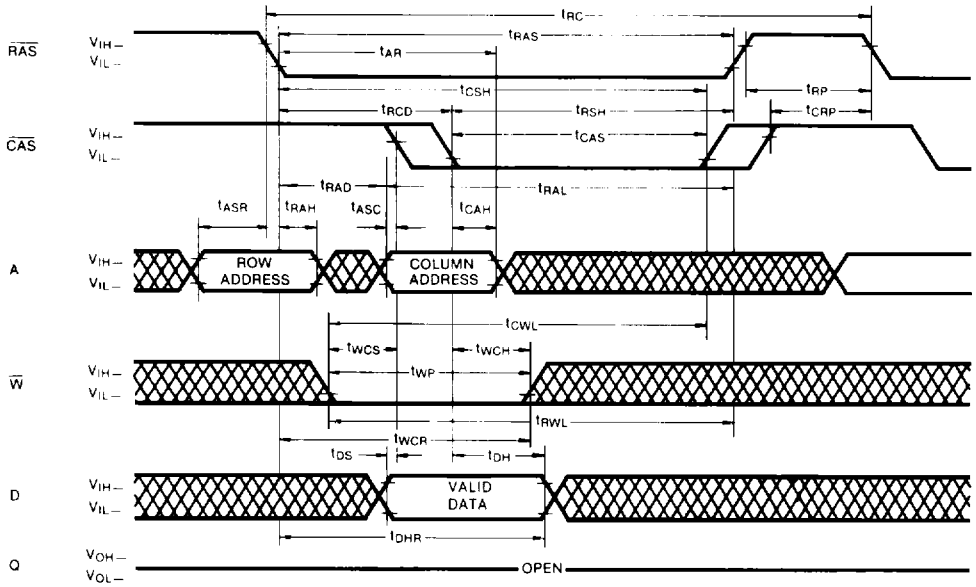
TIMING DIAGRAMS

READ CYCLE

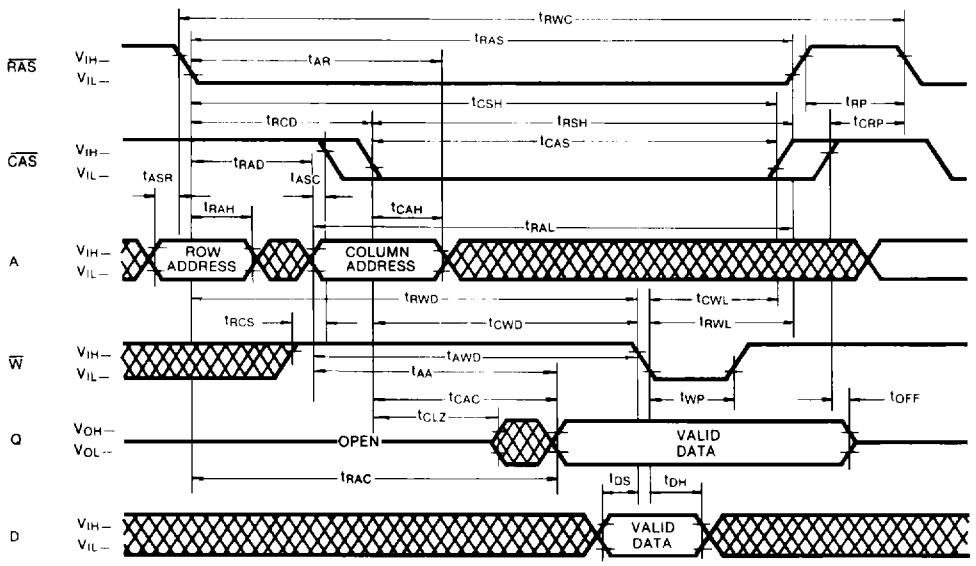


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

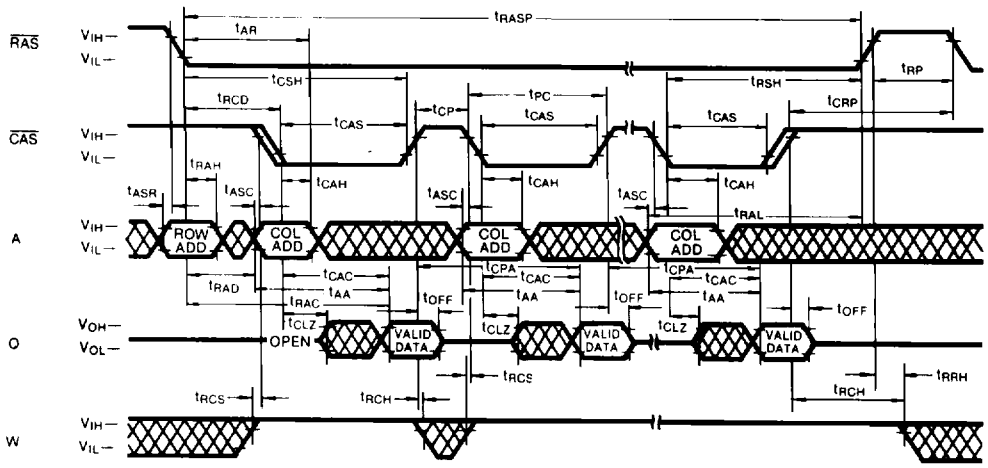


READ-WRITE/READ-MODIFY-WRITE CYCLE

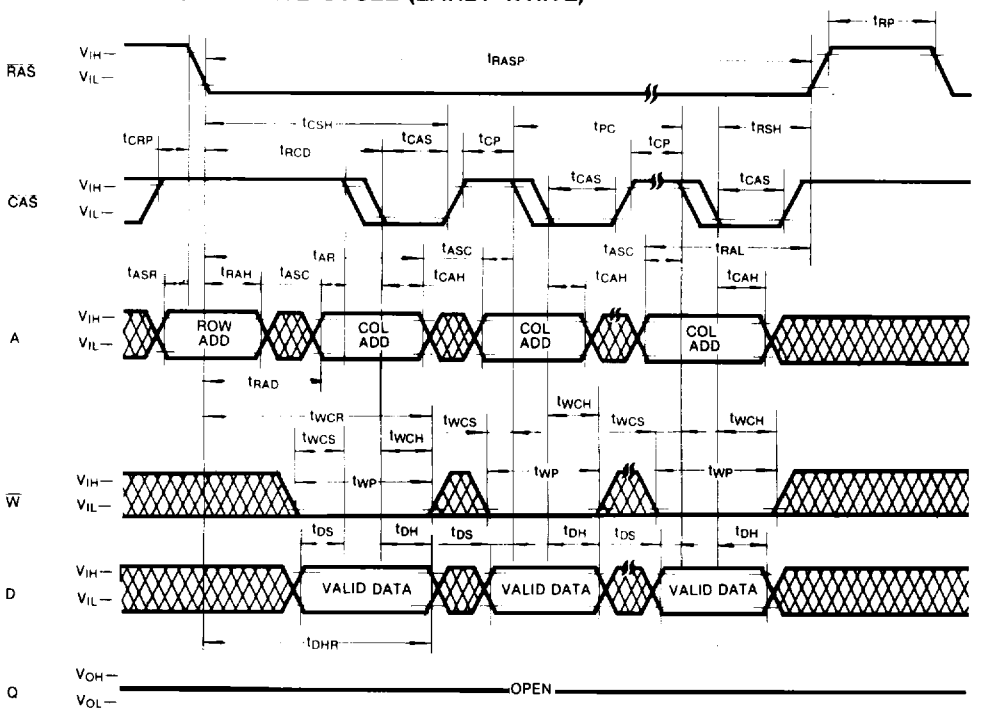


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

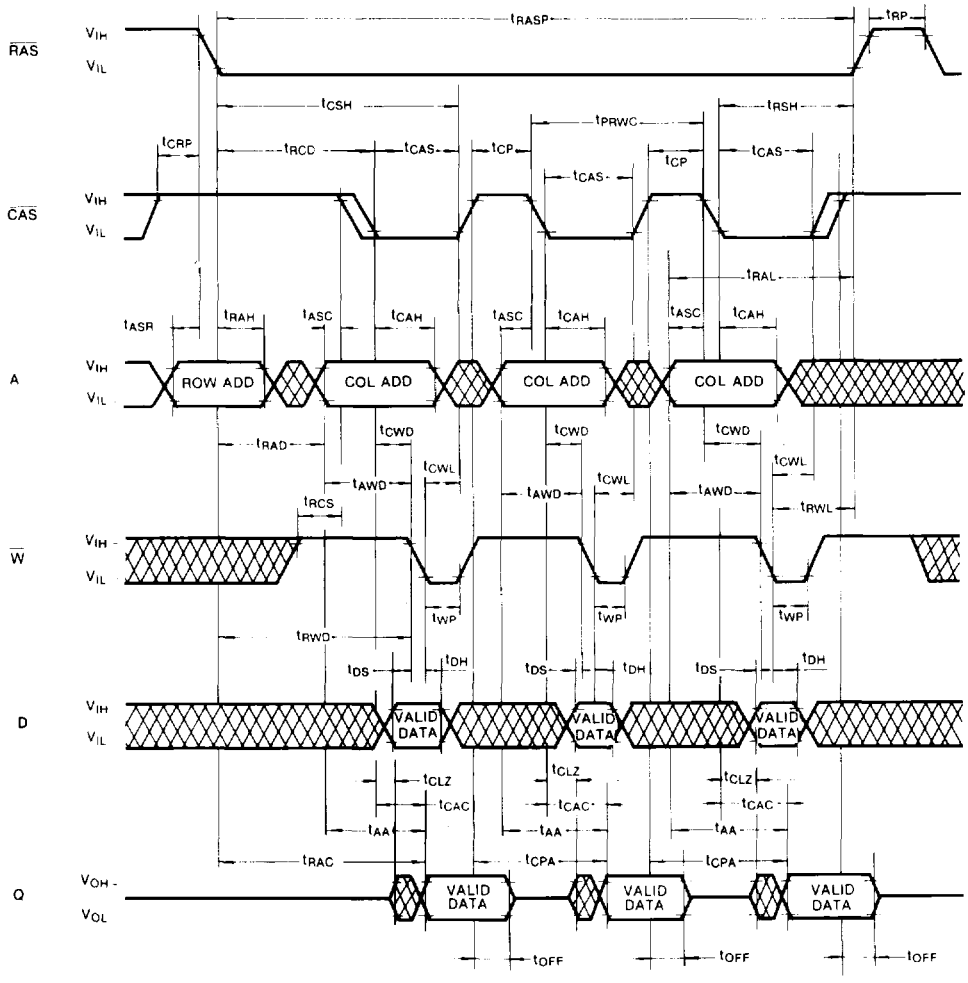


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

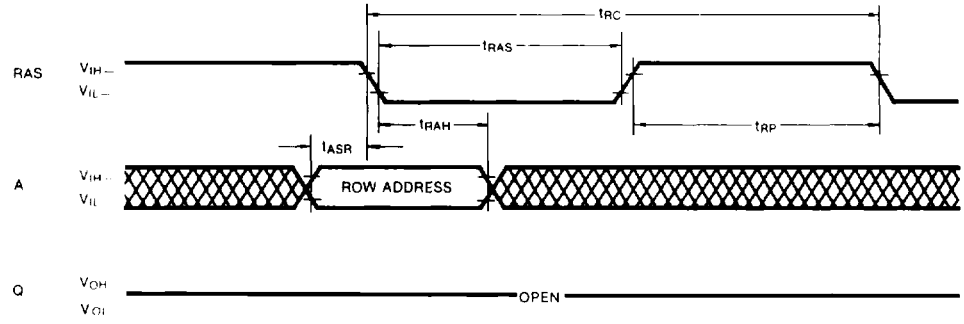
FAST PAGE MODE READ-WRITE CYCLE



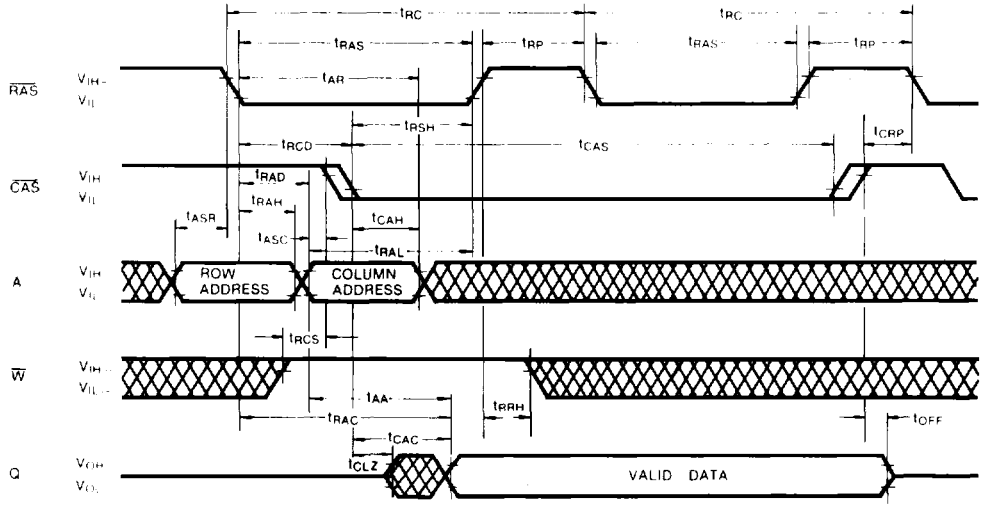
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_8 = Don't Care

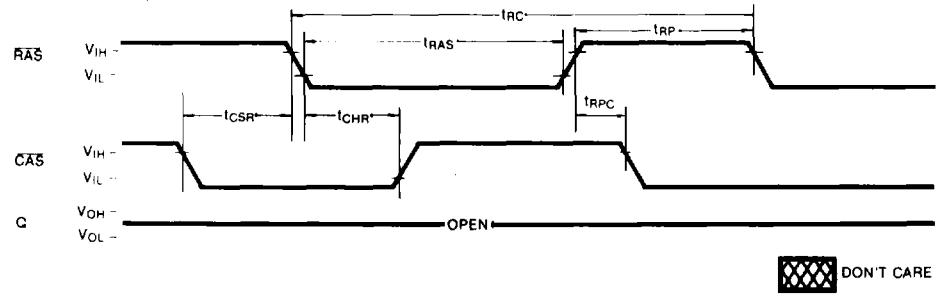


HIDDEN REFRESH CYCLE



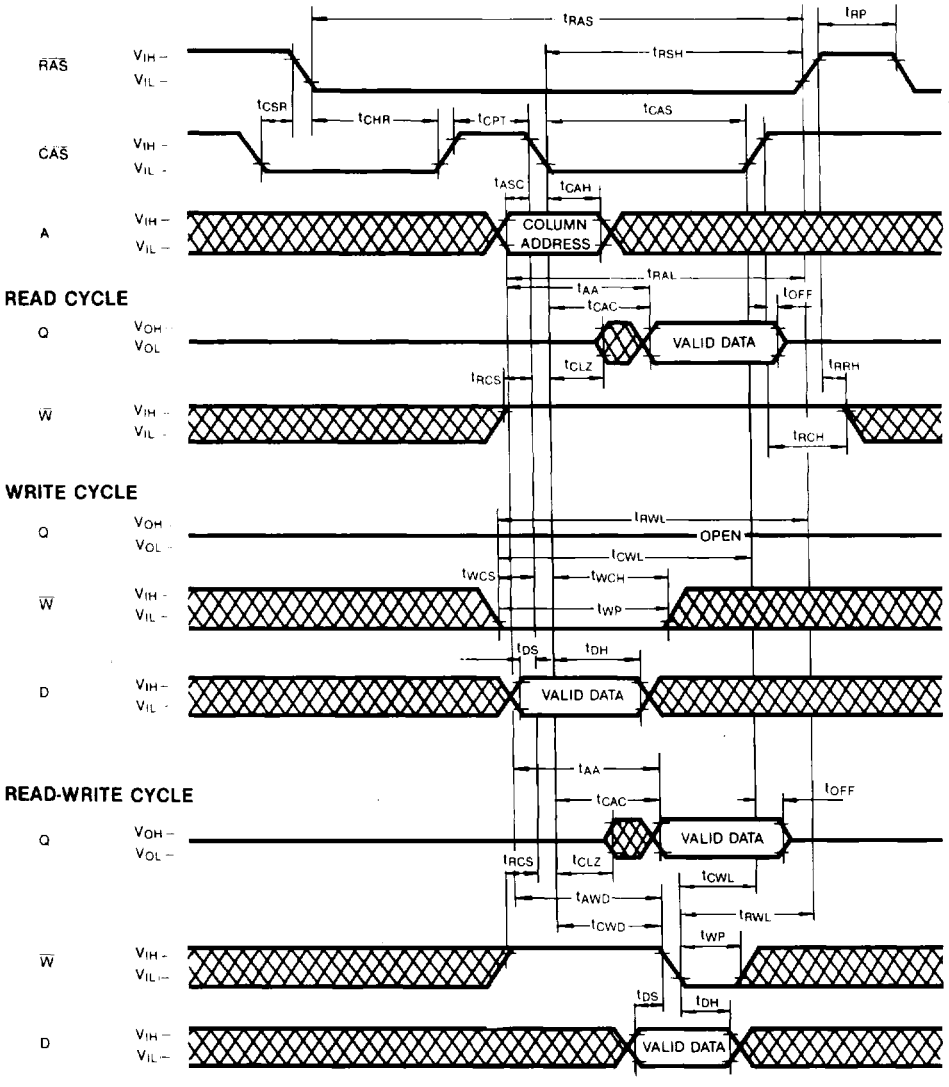
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address, $\overline{W}$, D = Don't Care



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DON'T CARE

DEVICE OPERATION

Device Operation

The KM41C256 contains 262,144 memory locations. Eighteen address bits are required to address a particular memory array. Since the KM41C256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C256 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters t_{CWD} and t_{AWD}, are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C256 has a three-state output buffers which are controlled by $\overline{CAS}$. When either $\overline{CAS}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C256 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Refresh

The data in the KM41C256 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes

DEVICE OPERATION (Continued)

low. the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C256 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C 256 has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or readmodify-write cycles. As long as the applicable timingg requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 512 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A_0 through A_7 are supplied by the on-chip refresh counter. The A_8 bit is set High internally.

Column Address—Bits A_0 through A_8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested CAS-Before-RAS Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.

2. Write a test pattern of "lows" int the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)

3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.

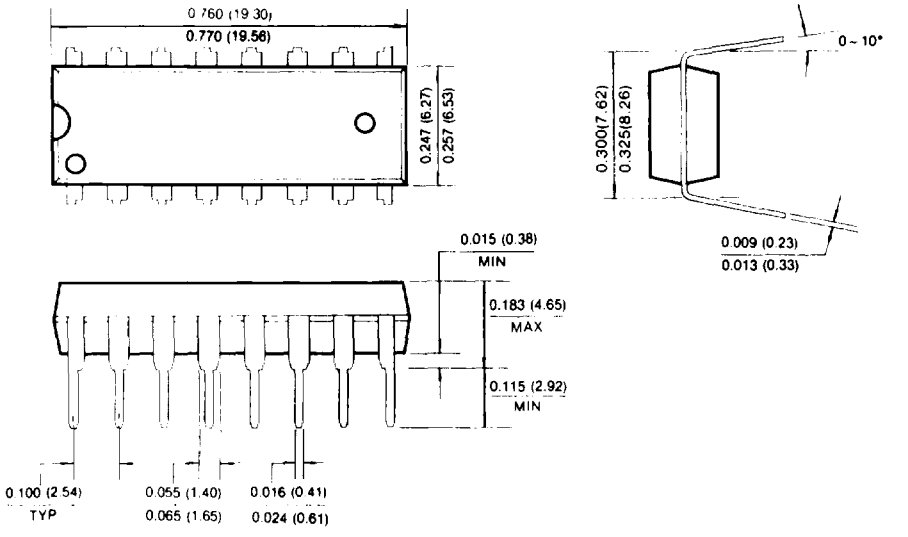
4. Read the "highs" written during step 3.

5. Complement the test pattern and repeat steps 2, 3 and 4.

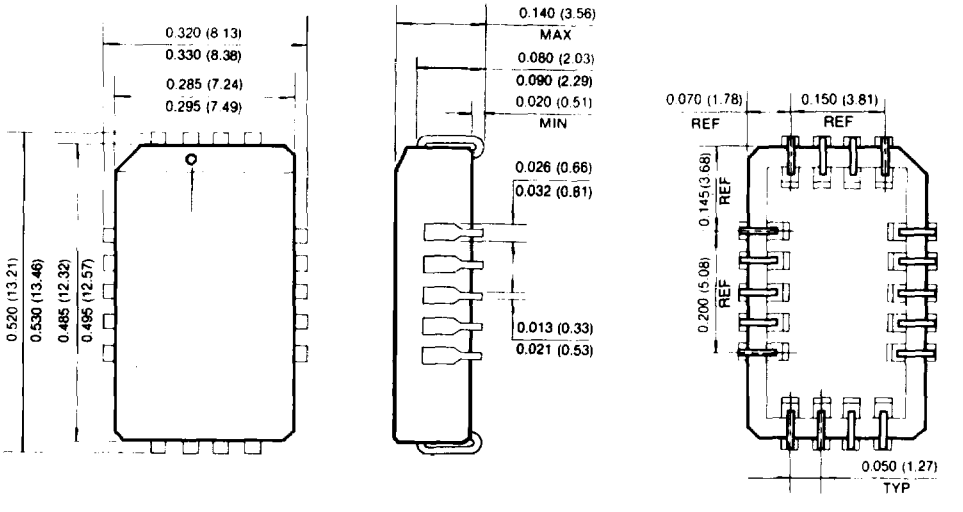
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)



18- LEAD PLASTIC CHIP CARRIER



PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

Units: Inches (millimeters)