1 Mega Byte

Fast Page Mode MSC 991100J3NS
1Mx9 DRAM SIMM, 1K Byte Refresh, 5.0V

GENERAL DESCRIPTION

The **MSC 991100J3NS** is a 1Mx9bits Dynamic RAM high density memory module. The **MSC 991100J3NS** consists of two CMOS 1Mx4bits DRAMs and one CMOS 1Mx1bit in 20-pin SOJ packages mounted on a 30-pin FR4 epoxy substrate. A 220nF decoupling capacitor is mounted on the printed circuit board for each DRAM. The **MSC 991100J3NS** is a Single In-line Memory Module with edge connections and is intended for mounting into 30-pin edge connector sockets.

FEATURES

- Performance Range:

	tRAC	tCAC	tRC
MSC 991100J3NS-6	60 nsec	15 nsec	110 nsec
MSC 991100J3NS-7	70 nsec	20 nsec	130 nsec

FEATURES (CONTINUED)

- FAST PAGE MODE
  45 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- $\overline{\text{CAS}}$ -before- RAS refresh capability
- $\overline{\text{RAS}}$ only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- 1024 cycles/16 msec refresh
- PCB: Height (500mil), single sided component

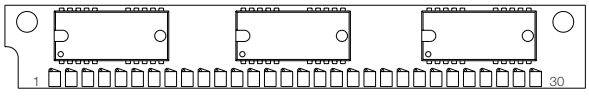
PIN CONFIGURATIONS

PIN	SYM	PIN	SYM
1	Vcc	16	DQ4
2	$\overline{\text{CAS}}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{\text{WE}}$
7	A2	22	Vss
8	A3	23	DQ6
9	Vss	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{\text{RAS}}$
13	DQ3	28	$\overline{\text{PCAS}}$
14	A6	29	PD
15	A7	30	Vcc

PIN NAMES

PIN NAME	FUNCTION
A0 - A9	Address Inputs
DQ0 - DQ7	Data IN/OUT
PD	Data In for Parity
PQ	Data Out for Parity
$\overline{\text{WE}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{PCAS}}$	$\overline{\text{CAS}}$ for Parity
Vcc	Power (+5.0V)
Vss	Ground
NC	No Connection

PIN CONNECTIONS (FRONT VIEW)



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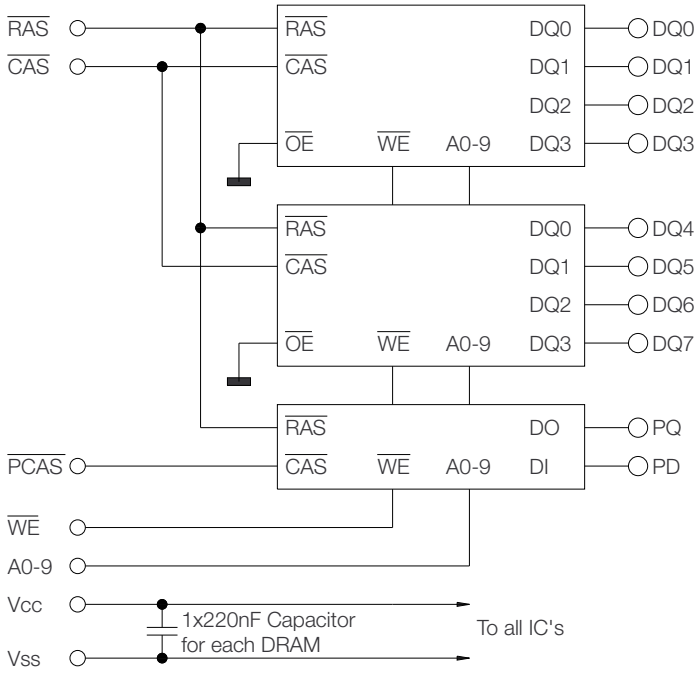
FUNCTIONAL BLOCK DIAGRAM



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Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	Vin, Vout	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1.0 to +7.0	V
Storage Temperature	Tstg	-40 to +110	°C
Power Dissipation	Pd	3.0	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

Recommended Operating Conditions (Voltage referenced to Vss, Ta = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc+1	V
Input Low Voltage	VIL	-1.0	-	0.8	V

DC and Operating Characteristics (Recommended operating conditions unless otherwise noted.)

Parameter	Part No	Symbol	Min	Max	Unit
Operating Current*	MSC 991100J3NS-6	ICC1	-	300	mA
($\overline{RAS}$, $\overline{CAS}$, Address cycling @ tRC=min.)	MSC 991100J3NS-7		-	270	mA
Standby Current		ICC2	-	6	mA
($\overline{RAS}$ = $\overline{CAS}$ = VIH)					
$\overline{RAS}$ -Only Refresh Current*	MSC 991100J3NS-6	ICC3	-	300	mA
($\overline{CAS}$ = VIH, $\overline{RAS}$ cycling @ tRC=min.)	MSC 991100J3NS-7		-	270	mA
Fast Page Mode Current*	MSC 991100J3NS-6	ICC4	-	200	mA
($\overline{RAS}$ = VIL, $\overline{CAS}$ cycling @ tPC=min.)	MSC 991100J3NS-7		-	170	mA
Standby Current		ICC5	-	3	mA
($\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = Vcc-0.2V)					
$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Current*	MSC 991100J3NS-6	ICC6	-	300	mA
($\overline{RAS}$ and $\overline{CAS}$ cycling @ tRC=min.)	MSC 991100J3NS-7		-	270	mA
Input Leakage Current (Any input 0≤VIN≤Vcc+0.5V,		II(L)	-30	30	µA
all other pins not under test = 0V.)					
Output Leakage Current		IO(L)	-3.75	3.75	µA
(Data out is disabled, 0V≤Vout≤Vcc)					
Output High Voltage Level (IOH=-5mA)		VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)		VOL	-	0.4	V

* Note: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum two times while RAS=VIL. In ICC4, address can be changed maximum once within one page mode cycle.

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Capacitance (Ta=25°C, f=1MHz)

Item	Symbol	Min	Max	Unit
Input Capacitance [A0 - A9]	CIN1	-	15	pF
Input Capacitance [$\overline{RAS}$]	CIN2	-	21	pF
Input Capacitance [$\overline{CAS}$]	CIN3	-	14	pF
Input Capacitance [PD, $\overline{PCAS}$]	CIN4	-	7	pF
Input Capacitance [DQ0 - DQ7]	CDQ	-	7	pF
Output Capacitance [PQ]	CQ	-	7	pF

AC Characteristics (0 °C ≤ Ta ≤ 70 °C, Vcc = 5.0 V ± 10 %, See notes 1,2.)

Standard Operation	Symbol	-50		-60		-70		-80		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write cycle time	tRC	-	-	110	-	130	-	-	-	nsec	
Access time $\overline{RAS}$	tRAC	-	-	-	60	-	70	-	-	nsec	3,4,11
Access time $\overline{CAS}$	tCAC	-	-	-	15	-	20	-	-	nsec	3,4,5
Address time from column address	tAA	-	-	-	30	-	35	-	-	nsec	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	-	-	0	-	0	-	-	-	nsec	3
Output buffer turn-off delay	tOFF	-	-	0	15	0	20	-	-	nsec	7
Transition time (rise and fall)	tT	-	-	3	50	3	50	-	-	nsec	2
$\overline{RAS}$ precharge time	tRP	-	-	40	-	50	-	-	-	nsec	
$\overline{RAS}$ pulse width	tRAS	-	-	60	10K	70	10K	-	-	nsec	
$\overline{RAS}$ hold time	tRSH	-	-	15	-	20	-	-	-	nsec	
$\overline{CAS}$ hold time	tCSH	-	-	60	-	70	-	-	-	nsec	
$\overline{CAS}$ pulse width	tCAS	-	-	15	10K	20	10K	-	-	nsec	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	-	-	20	45	20	50	-	-	nsec	4
$\overline{RAS}$ to column address delay time	tRAD	-	-	15	30	15	35	-	-	nsec	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	-	-	5	-	5	-	-	-	nsec	
Row address set-up time	tASR	-	-	0	-	0	-	-	-	nsec	
Row address hold time	tRAH	-	-	10	-	10	-	-	-	nsec	
Column address set-up time	tASC	-	-	0	-	0	-	-	-	nsec	
Column address hold time	tCAH	-	-	15	-	15	-	-	-	nsec	
Column address hold referenced to $\overline{RAS}$	tAR	-	-	50	-	55	-	-	-	nsec	6
Column address to $\overline{RAS}$ lead time	tRAL	-	-	30	-	35	-	-	-	nsec	
Read command set-up time	tRCS	-	-	0	-	0	-	-	-	nsec	
Read command hold referenced to $\overline{CAS}$	tRCH	-	-	0	-	0	-	-	-	nsec	9
Read command hold referenced to $\overline{RAS}$	tRRH	-	-	0	-	0	-	-	-	nsec	9
Write command hold time	tWCH	-	-	10	-	10	-	-	-	nsec	
Write command hold referenced to $\overline{RAS}$	tWCR	-	-	45	-	50	-	-	-	nsec	6
Write command pulse width	tWP	-	-	10	-	10	-	-	-	nsec	
Write command to $\overline{RAS}$ lead time	tRWL	-	-	15	-	15	-	-	-	nsec	
Write command to $\overline{CAS}$ lead time	tCWL	-	-	15	-	15	-	-	-	nsec	

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AC Characteristics (0 °C ≤ Ta ≤ 70 °C, Vcc = 5.0 V ± 10 %, See notes 1,2.)

Standard Operation	Symbol	-50		-60		-70		-80		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data-in set-up time	tDS	-	-	0	-	0	-	-	-	nsec	10
Data-in hold time	tDH	-	-	15	-	15	-	-	-	nsec	10
Data-in hold referenced to $\overline{RAS}$	tDHR	-	-	50	-	55	-	-	-	nsec	6
Refresh period	tREF	-	-	-	16	-	16	-	-	msec	
Write command set-up time	tWCS	-	-	0	-	0	-	-	-	nsec	8
$\overline{CAS}$ set-up time (C-B-R-refresh)	tCSR	-	-	10	-	10	-	-	-	nsec	
$\overline{CAS}$ hold time (C-B-R-refresh)	tCHR	-	-	10	-	15	-	-	-	nsec	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	-	-	5	-	5	-	-	-	nsec	
Access time from $\overline{CAS}$ precharge	tCPA	-	-	-	35	-	40	-	-	nsec	3
Fast Page mode cycle time	tPC	-	-	40	-	45	-	-	-	nsec	
$\overline{CAS}$ precharge time (Fast Page)	tCP	-	-	10	-	10	-	-	-	nsec	
$\overline{RAS}$ pulse width (Fast Page)	tRASP	-	-	60	100K	70	100K	-	-	nsec	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	-	-	35	-	40	-	-	-	nsec	
$\overline{WE}$ to$\overline{RAS}$ precharge time (C-B-R refresh)	tWRP	-	-	10	-	10	-	-	-	nsec	
$\overline{WE}$ to $\overline{RAS}$ hold time (C-B-R refresh)	tWRH	-	-	10	-	10	-	-	-	nsec	
$\overline{CAS}$ precharge (C-B-R counter test)	tCPT	-	-	20	-	25	-	-	-	nsec	

Notes

1. An initial pause of 200 µsec is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH (min) and VIL (max) and are assumed to be 5 nsec for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 110pF.

4. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only. If tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.

5. Assumes that tRCD ≥ tRCD (max).

6. tAR, tWCR, tDHR are referenced to tRAD (max).

7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.

8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS (min) the cycle is an early write cycle and the data out pin will remain high impedance for duration of the cycle.

9. Either tRCH or tRRH must be satisfied for a read cycle.

10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

11. Operation within the tRAD (max) limit insure that tRAC (max) can be met. tRAD (max) is specified as reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.

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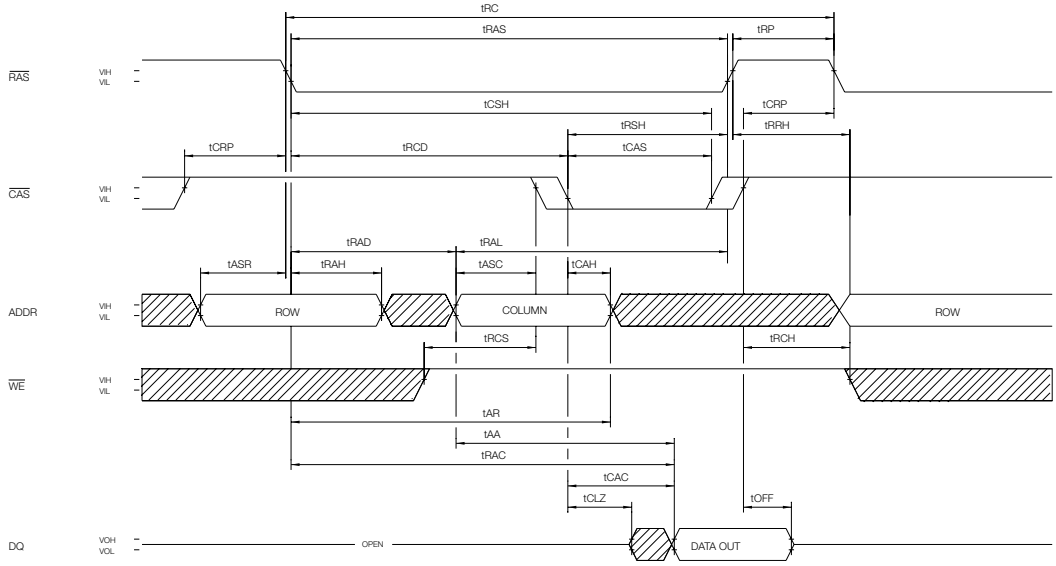
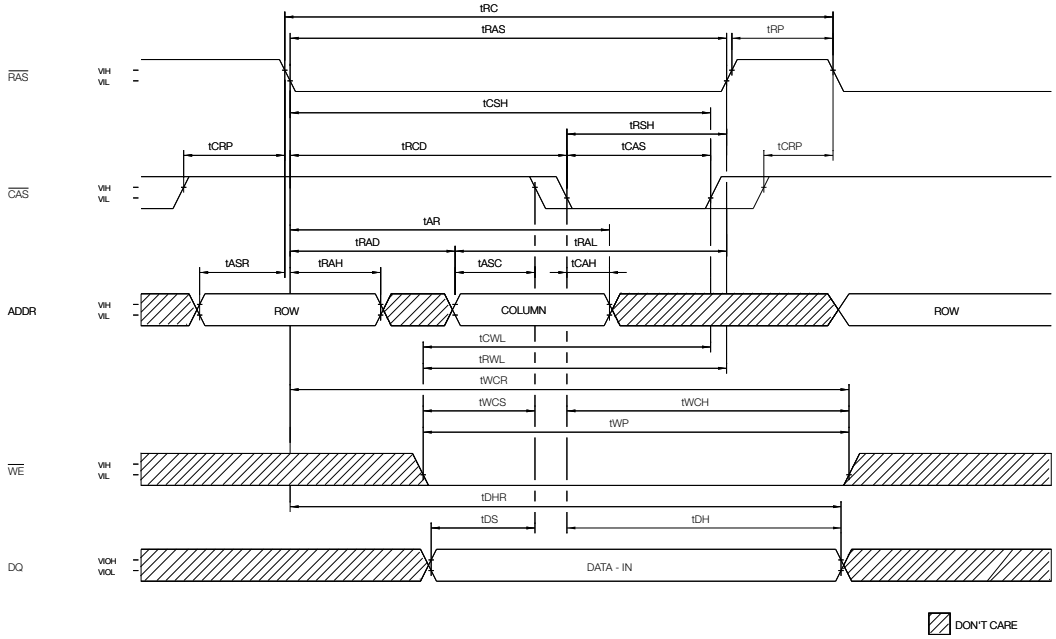
Timing Diagram

READ CYCLE



WRITE CYCLE (EARLY WRITE)

(NOTE: Dout = Open)



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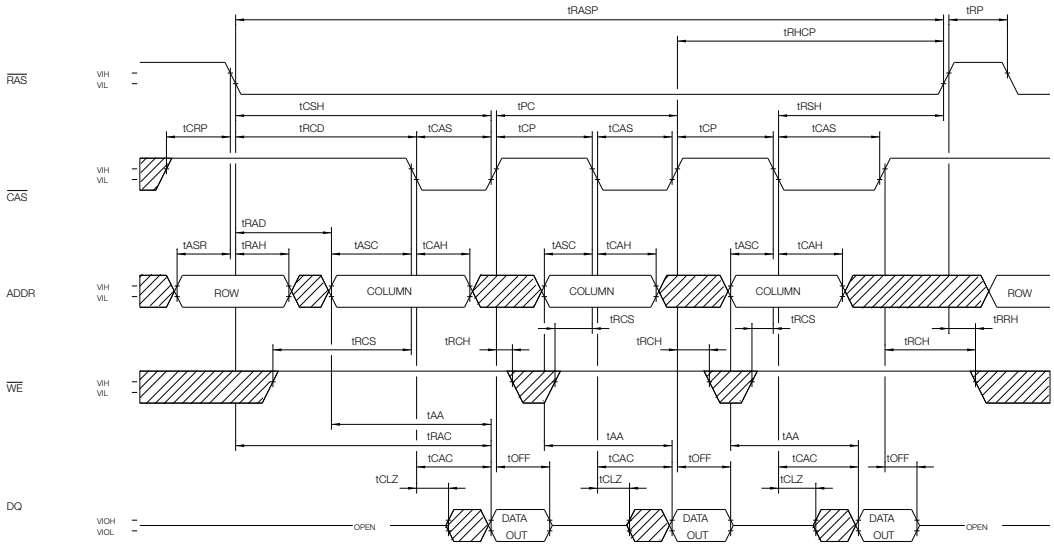
Timing Diagram

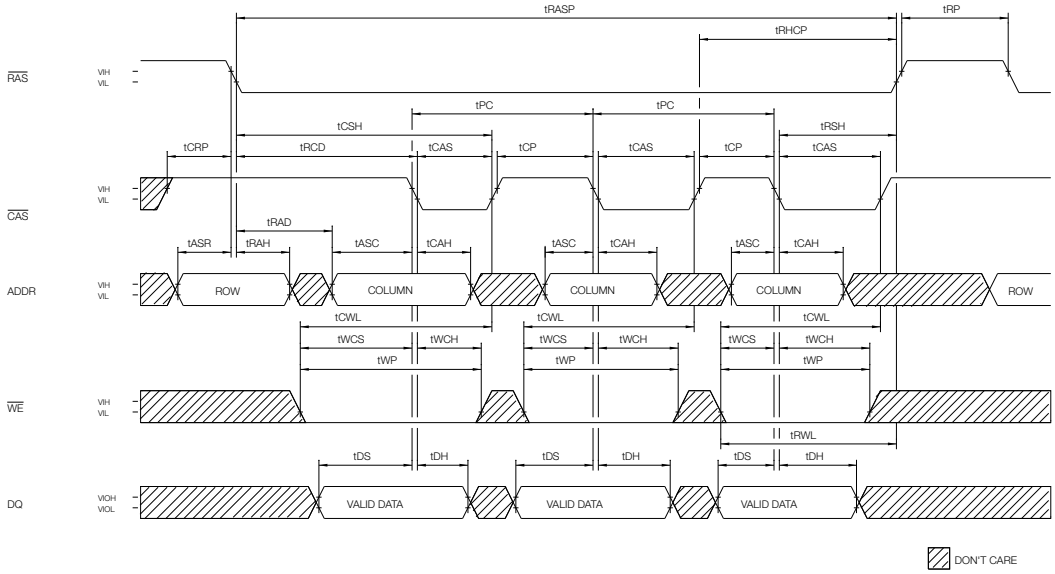
FAST PAGE READ CYCLE

(NOTE: Dout = Open)



FAST-PAGE-WRITE CYCLE (EARLY WRITE)

(NOTE: Dout = Open)



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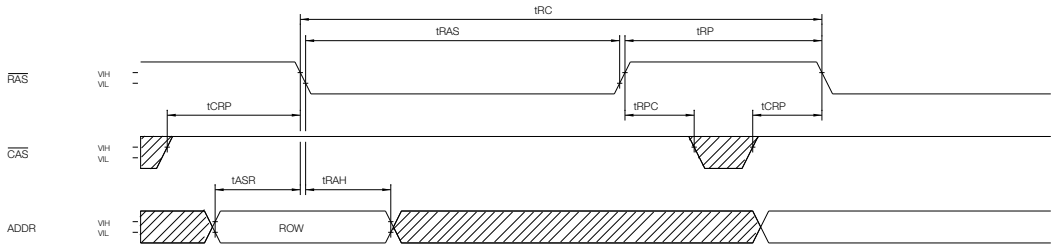
Timing Diagram

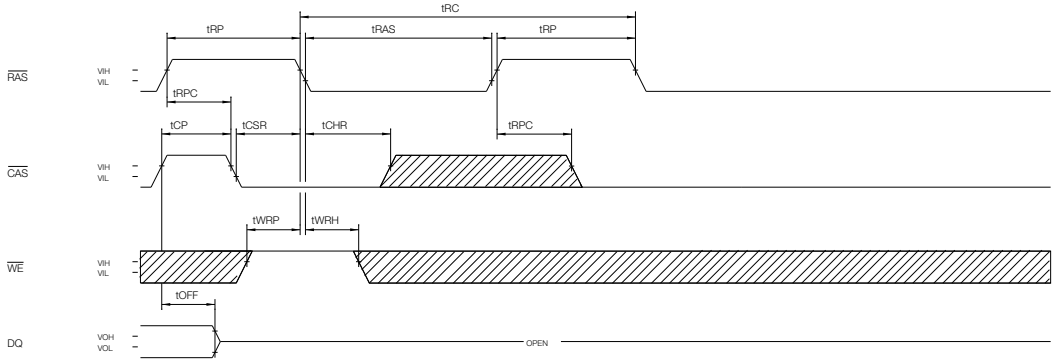
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

(NOTE: $\overline{\text{WE}}$, $\overline{\text{OE}}$, DIN = Don't care, Dout = Open)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

(NOTE: $\overline{\text{WE}}$, $\overline{\text{OE}}$, ADDR = Don't Care)



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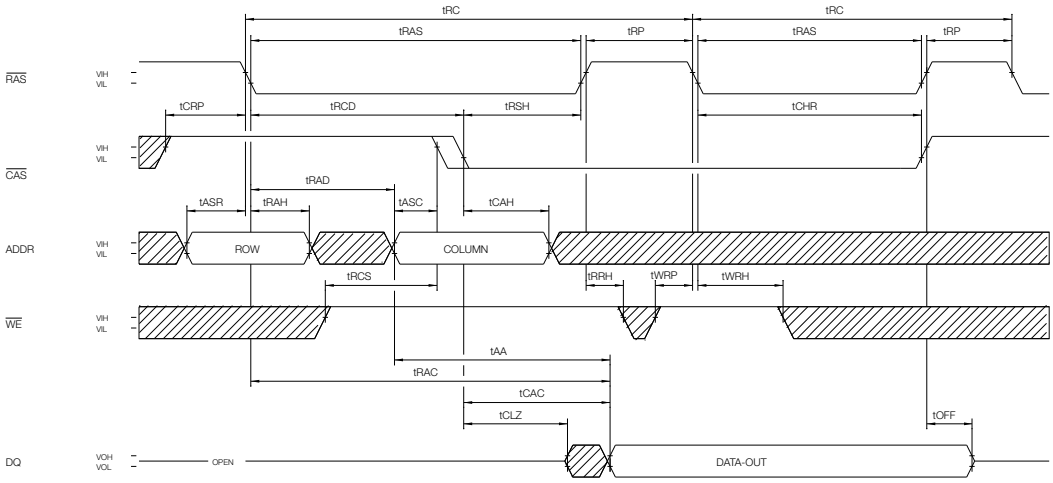
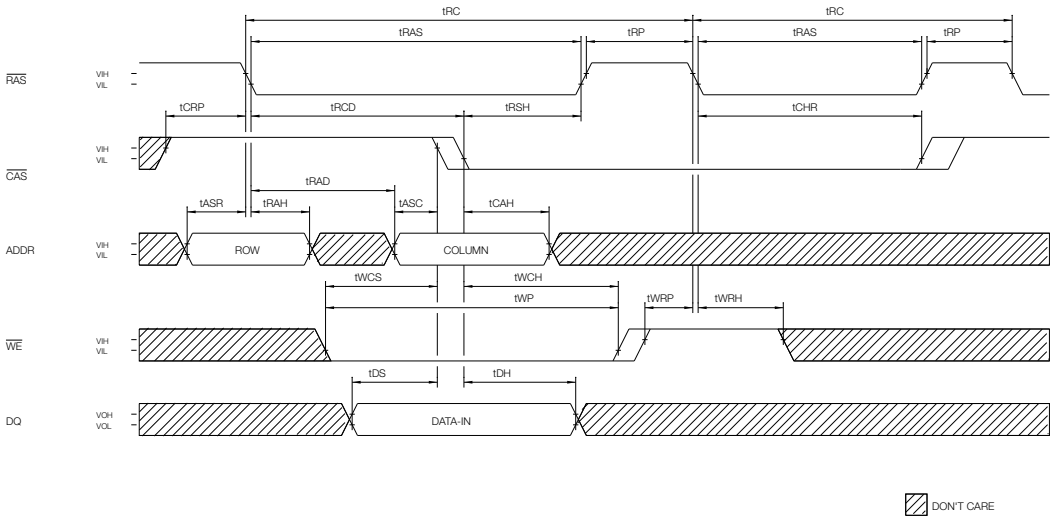
Timing Diagram

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

(NOTE: DOUT = OPEN)



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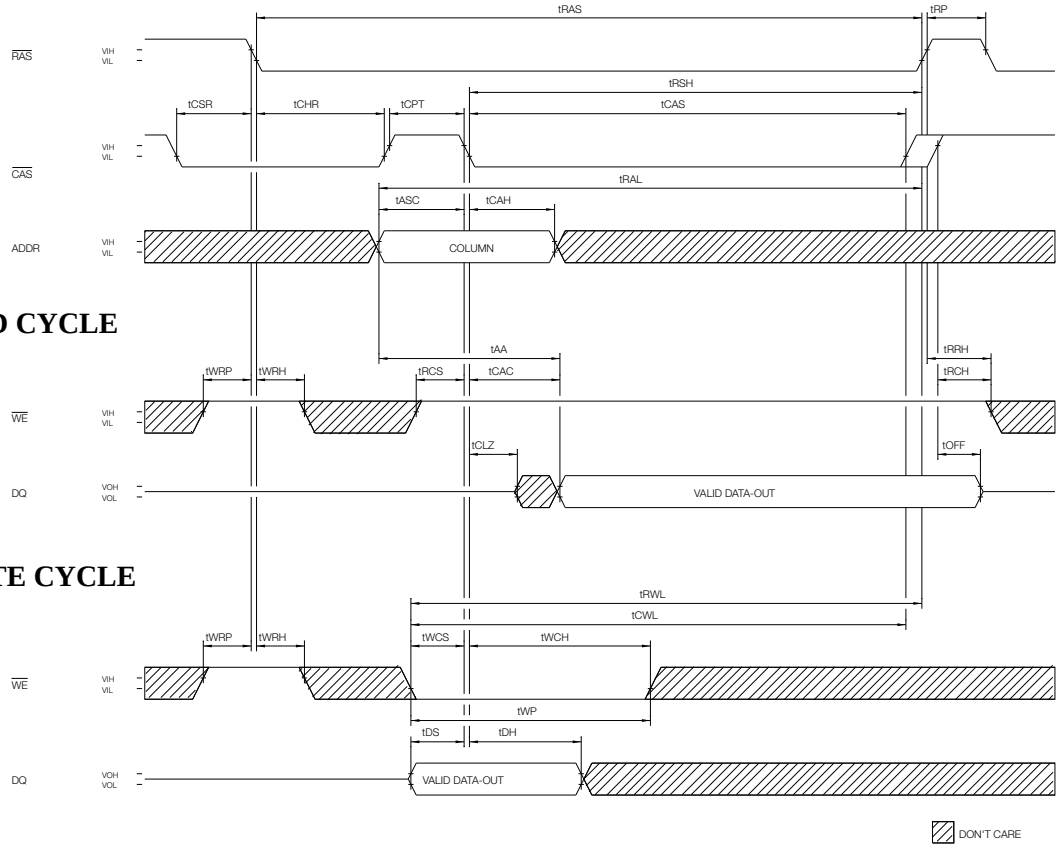
Timing Diagram

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



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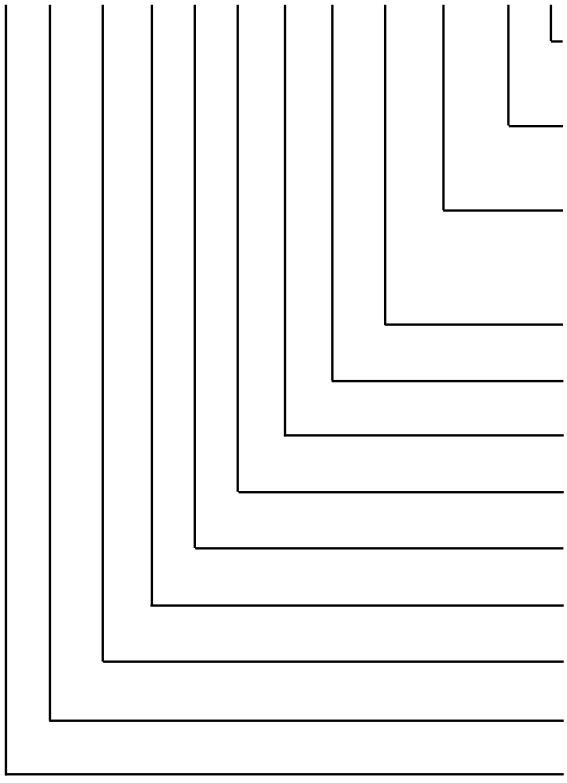
ORDERING INFORMATION

MSC 9911 F G H I J K L M N - O P



- **„“ = Normal Power**
  L = Low Power
- **6 = 60 nsec**
  x = xx nsec
- **„“ = SIMM-connector (tin)**
  G = SIMM-connector (gold)
  P = SIP-connector (pin)
- **S = single side Assembled**
- **N = 500 mil Module height**
- **„“ = Without Option**
- **3 = 300 mil IC Package form**
- **J = SOJ IC package**
- **0 = Fast Page with PD**
- **0 = 5.0 V**
- **„“ = Single Bank**
- **1 = 1 K Byte refresh**

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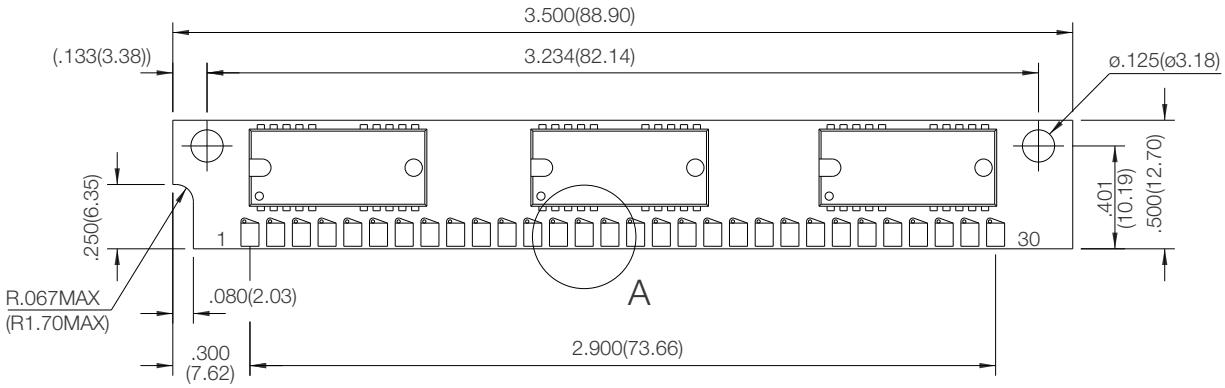
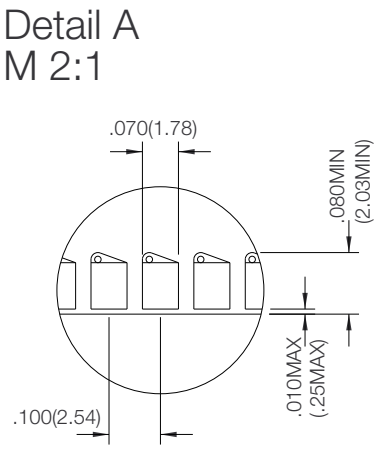
PACKAGE DIMENSIONS

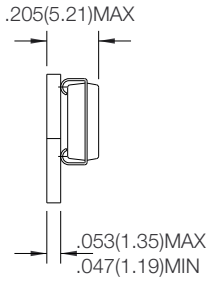
Front View



Detail



Side View



Tolerances: ±.005(.13) unless otherwise specified
All dimensions in inches (millimeters) MAX/MIN or typical where noted.

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